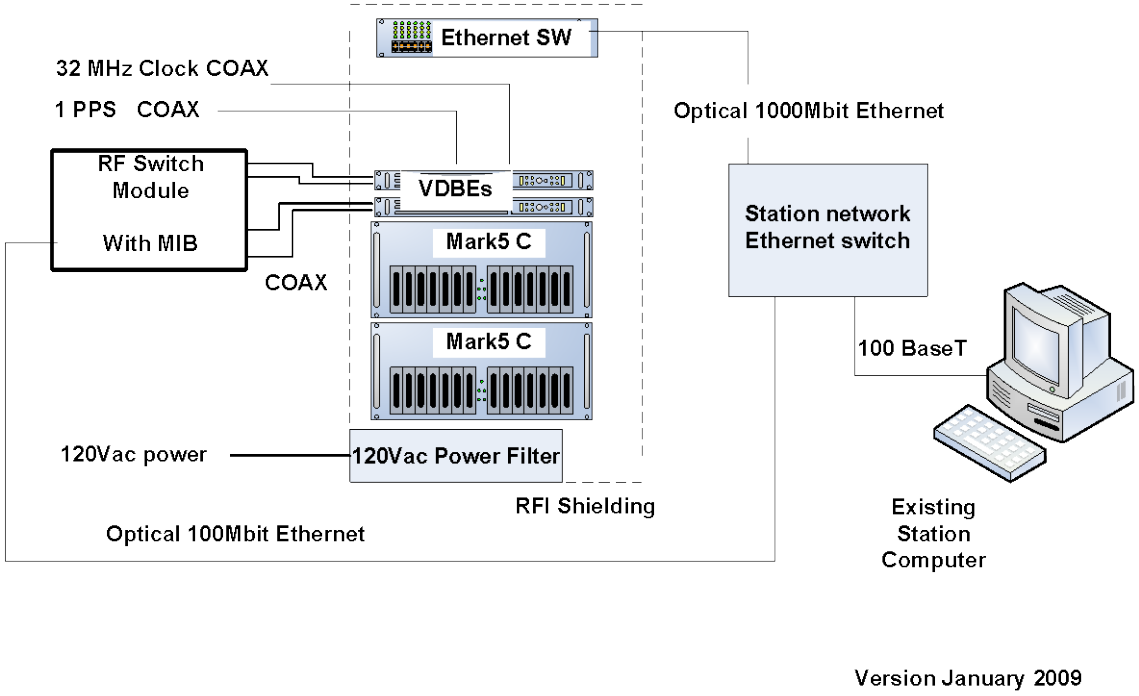
# VLBA Sensitivity Upgrade: Overview / Hardware /Software / Targets

Jon Romney

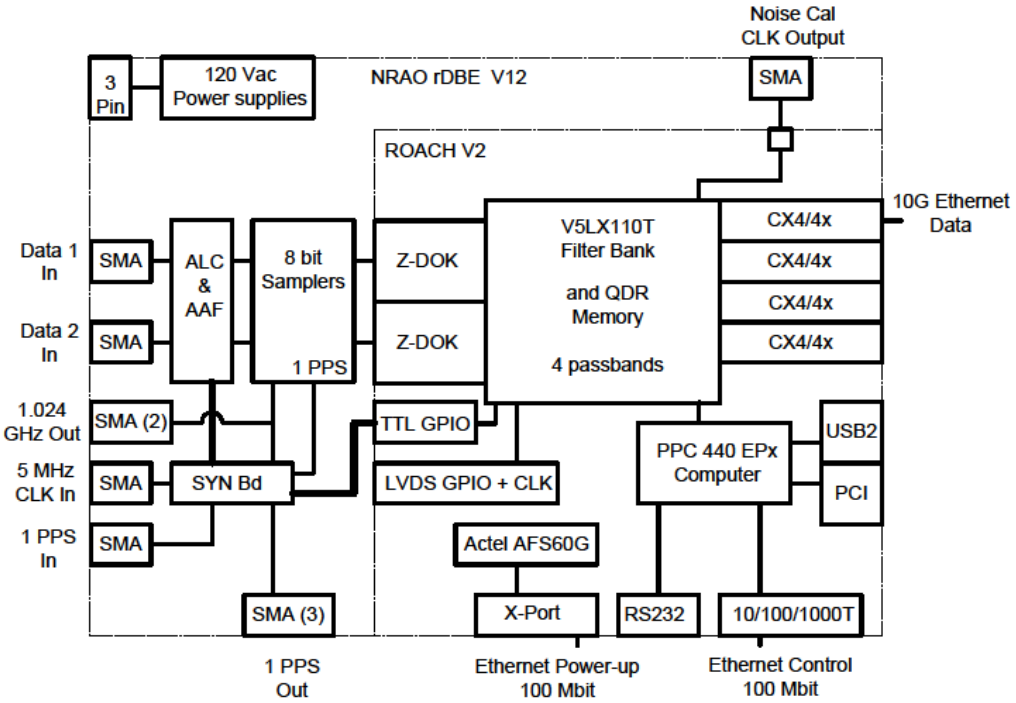
Software Group Meeting

2010 February 9

# Overview of New VLBA Station Equipment



# ROACH Digital Back-End (RDBE) – Detailed View



# Recent RDBE Workshop at Haystack Observatory

## NRAO Participants

Miguel Guerra & Matt Luce.

## Primary Achievements

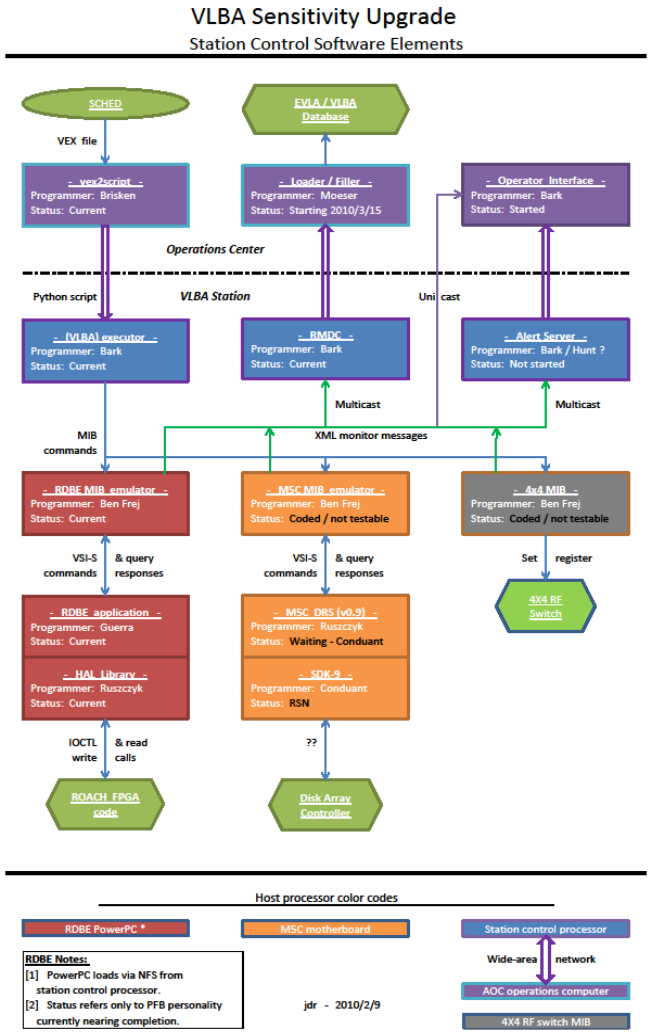
Integration of ML's "Julian Clock Module" into PFB FPGA system.

End-to-end demonstration, at full 2-Mbps output data rate.

- Written onto Mark 5C and correlated on Haystack software correlator.
- Written onto system disk and analyzed using Matlab.

Continued planning for Level Control.

# Station Control Software Overview Diagram



# Project Schedule — Software Considerations

## Most Elements are "Current"

- Basic software structure present and functional.
- Many (but not necessarily all) specific functions implemented.
- Able to add new functions expeditiously, as requested from other elements.
- Staff (including Haystack personnel) working well together to communicate new requirements.

## A Few Exceptions

- Most in Mark 5C area.
  - Dependent on outside contractors:
    - Conduant SDK-9 & Haystack DRS-0.9.
  - MIB code cannot be tested.
- 4X4 RF switch MIB code also waiting for hardware.

# RDBE / PFB Support Progressing Well

Paced primarily by FPGA code development.

*Implication for overall project schedule: should be OK to target completion of support software ~ 1 month after FPGA code.*

# Complete Test System Being Assembled

# Software-Related and Essential Hardware Milestones

| VLBA Sensitivity Upgrade Targets | | | |
|---|---|---|---|
| Abstract for Software Group Meeting | | | |
| Target Date | Sub-Project | Description | Notes |
| DONE | DBE | Full-rate data path demo (~500 packets, PFB) | |
| DONE | DBE | NRAO Julian Clock Module (JCM) ready | |
| PENDING | DBE | PFB FPGA firmware ready | Update after SPFDR |
| 2010 Feb 03 | M5C | SDK 9 control software delivered | Waiting for Conduant |
| 2010 Feb 05 P | | VLBA station M&C upgrade document | |
| 2010 Feb 10 | DBE | Signal processing Functional Design Review | |
| 2010 Feb 17 | M5C | DRS control app 0.9 & documentation ready | SDK 9 + 2w |
| 2010 Mar 03 | M5C | Acceptance tests complete | DRS 0.9 + 2w |
| 2010 Apr 03 | | Station control software ready (PFB) | |
| 2010 Apr 03 | M5C | Initial operator GUI ready | Acceptance + 1m |
| 2010 Apr 15 P | | Station monitor data path complete | |
| PENDING | DBE | DDC FPGA firmware ready | Update after SPFDR |
| 2010 Aug 12 | | Sensitivity Upgrade operational at 2 Gbps | |


# Thank You