



ALMA Study Project

PMD-365: Recommended ALMA Hardware Changes Required by the Correlator Upgrade

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Recommended ALMA Hardware Changes Required by the Correlator Upgrade


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Abstract

Larger bandwidths and gains in ALMA sensitivity require not only a correlator upgrade but also upgrades of the receivers, digitizers, data transport subsystem and software. Ideally, these upgrades should be coordinated although studies and prototyping could progress separately in different groups until the full benefit of all upgrades is scheduled. This report addresses some of the questions related to the ALMA hardware changes required by the correlator upgrade which consists in doubling the processed bandwidth and enhancing the spectral resolution (x8). The correlator upgrade and the need for faster digitizers have an impact on data capture and baseband extraction, transmission of higher data rates in the optical fiber -especially if 4-bit digitizers are considered- and, at the fiber reception end, on bit alignment and data decoding. In addition to the design of a new digitizer assembly, new designs are required for the digital data transmission card (DTX) and, in the correlator Station electronics racks, for the data reception card (DRX) and the digital filtering card which extracts sub-channels from each baseband. Improved Front-End receivers will also have to be designed to match the proposed correlator upgrade. Our main goals here are threefold: identify the ALMA subsystems impacted by the correlator enhancement; briefly recall some features of these subsystems; give first details, without pretending to be exhaustive, on the hardware changes resulting from the correlator upgrade. General purpose or specific recommendations for the hardware system changes are suggested and summarized at the end of this work. Among those, perhaps the most important ones are: digitize the full IF band

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with 3 or 4 bits, flexible extraction of basebands in a new DTX module and implement DRX and digital filtering functions in a same card.

Revision History

2016-November-14: Initial Issue

2016-December-21: Various minor corrections throughout the document. Incorporate new considerations on interface fibers (§3.4) and active WDM system (§3.3 and 3.4).


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1 Introduction

The ALMA 64-antenna correlator upgrade aims to double the processed bandwidth and to enhance the spectral resolution by a factor of 8. The upgrade could begin with the resolution increase which requires a new correlator chip (the ALMA2 ASIC) and a new correlator card design, and later be followed by doubling the bandwidth. The ‘System Test Plan’ prepared during this Study describes the proposed strategy to implement and test the correlator system changes.

This report addresses the question of further changes that are required to take advantage of the full correlator upgrade. We identify the ALMA subsystems impacted by the correlator upgrade and present a first simple description of changes concerning the Front-End, Back-End and the digital data transmission (DTS) subsystems. The new correlator Station electronics cards and the new correlator chip and cards are described elsewhere. However, we include here (without giving design details) the new Tunable Filter Bank (TFB) card and its links to the DTS receiver card and the correlator Station card. This report also suggests recommendations to accommodate the bandwidth doubling.

The impact of the correlator upgrade on the software, either CASA software (observing tool, data analysis, archiving) or other softwares (hardware set-up or on-line and atmospheric calibration) is not discussed in this report.

2 Acronyms

A list of the acronyms used in this document is given below.

ADC	Analog-to-Digital Converter
ALMA	Atacama Large Millimeter/submillimeter Array
ALMA2	Name of the ASIC for the correlator upgrade
AOS	Array Operation Site (of the ALMA Observatory)
ASIC	Application-Specific Integrated Circuit
DRX	Data Receiver (part of DTS)
DTX	Data Transmitter (part of DTS)
DTS	Data Transmission System
DWDM	Dense Wavelength-Division Multiplexer
ESO	European Southern Observatory
FOAD	Fiber Optic EDFA/DWDM Demultiplexer
FOM	Fiber Optic DWDM Multiplexer



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FPGA	Field-programmable Gate Array
IF	Intermediate Frequency
IFDC	IF Downconverter in IFP subsystem
IFP	IF Processor subsystem
IPT	Integrated Product Team
LAB	Laboratoire d'Astrophysique de Bordeaux, Univ. de Bordeaux
LRU	Line Replaceable Unit
NRAO	National Radio Astronomy Observatory
OSF	Operations Support Facility (of the ALMA Observatory)
SC	Station Card
TE	Timing Event
TFB	Tunable Filter Bank

3 Hardware Changes Required by the Correlator Upgrade

The ALMA subsystems impacted by the 64-antenna correlator upgrade are listed in Table 1. Several of these subsystem changes are being studied within the ALMA community and prototypes may become available in a near future (e.g. new receivers for some ALMA bands and new digitizers). Simultaneous readiness of all changes is not necessarily needed so that, once development funds have been granted, design, verification in the field and commissioning are possible in a progressive manner. However, when all changes are validated in laboratory test stands or in the field, it would be useful to investigate the programmatic efficiency of simultaneously implementing the correlator doubling bandwidth upgrade and the new digitizer and digital transmission upgrades. We describe below each element in Table 1, except software not discussed in this report.

Table 1. Impact of 64-antenna correlator upgrade on ALMA subsystems

Impacted Element	ALMA Subsystem	Remarks
Receiver	Front-End	Larger instantaneous bandwidth required
Digitization & IFDC	Back-End Digitizer & IFDC	Faster digitizers required & digitize full IF range desirable
DTX and fiber optic mux/demux	Data Transmission System	New DTX & DWDM required
DRX Card and TFB Card	Correlator	DRX & TFB functions in a single card desirable
<i>Software</i>		<i>Not discussed here</i>



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Fig. 1, extracted from Ref [1], summarizes the impact of bandwidth doubling on the ALMA antenna electronics, DTS and correlator ‘Station’ and ‘Baseline’ electronics. The Front-End receivers not shown in Fig. 1 are discussed in the next Section.

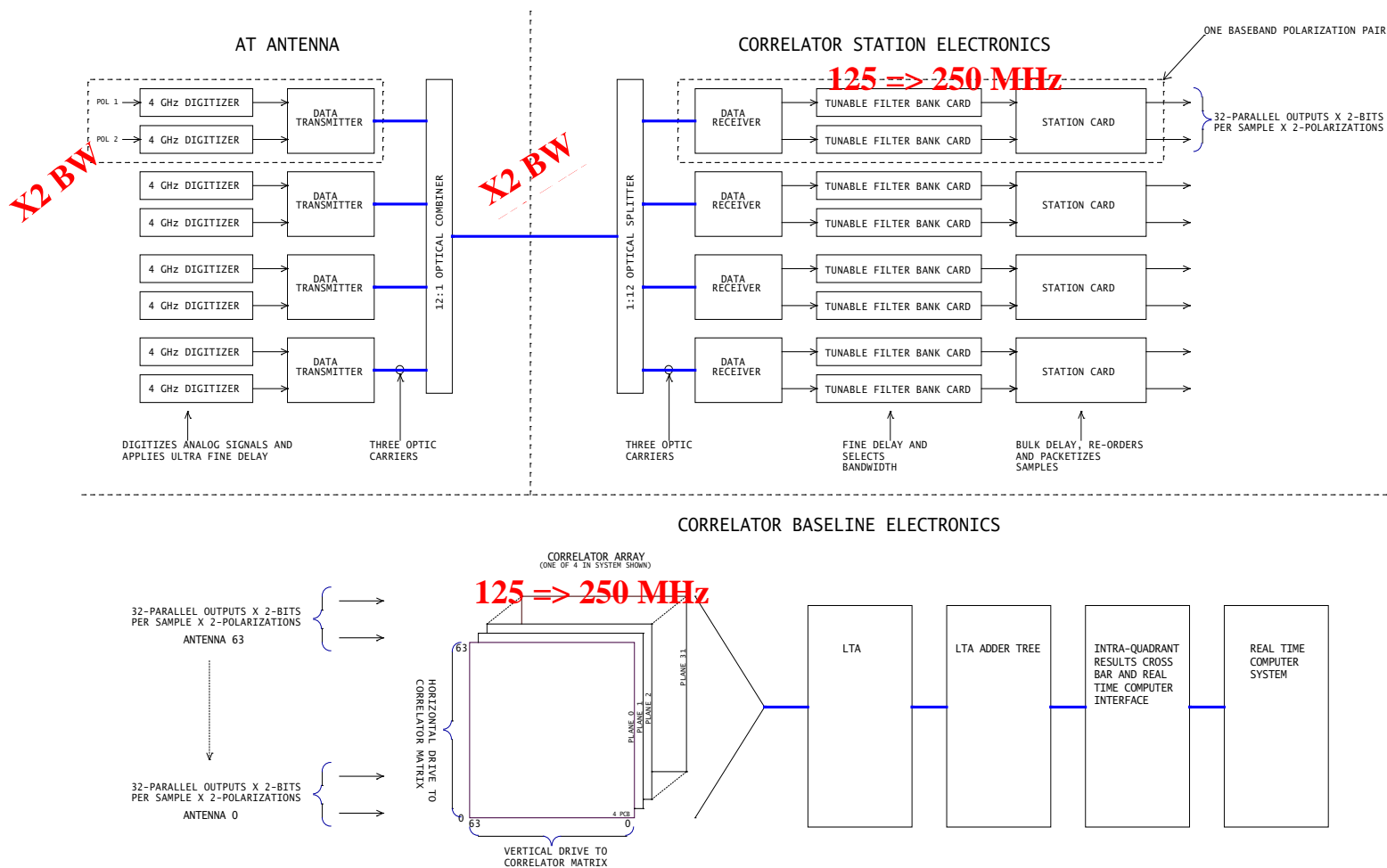


Figure 1 Correlator Block Diagram

Fig. 1: Impact of bandwidth doubling at the antenna and on the correlator Station and Baseline electronics

3.1 Improved Receivers

In order to match the correlator bandwidth upgrade, receivers with wider instantaneous bandwidths will have to be designed for at least some ALMA bands. Larger bandwidths



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are a high priority for future ALMA science projects in both line and continuum observing modes and are recommended in the road map document for developing ALMA. Doubling the bandwidth of 2SB receivers will provide 8 GHz USB and LSB bandwidths from the current IF 4-12 GHz range (instead of the current 4 GHz bandwidth in e.g. 4-8 GHz of the IF range for ALMA Bands 3 and 7 or 6-10 GHz for Band 6).

It is worth noting that,

(a) If the IF range of a new receiver design would be expanded beyond 4-12 GHz for scientific reasons, it would not match the planned correlator bandwidth doubling which would then process less than the available broader IF range. The correlator upgrade discussed here, which we view as an intermediate stage towards a future next generation correlator, does not need an IF range larger than the current 4-12 GHz.

(b) Designing new, broader bandwidth receivers may impact the design of the current Front-End first LO driver in the warm cartridge. This would not have any impact on the correlator upgrade.

(c) Designing new broad band receivers and on-site commissioning tasks can be decoupled from the baseline correlator upgrade tasks. However, ultimately, at least one new receiver is needed to verify that the upgraded correlator processes twice the current system bandwidth. Verification of the receiver-correlator enhanced bandwidth matching and processing can be made in any of the ALMA bands. First tests with one of the most currently used ALMA bands (i.e. bands 3, 6 or 7) would be fine.

3.2 Broad Band Digitization and New IFDC

Doubling the correlator bandwidth requires to design faster digitizers and to modify the analog IF downconverter (IFDC) subsystem. The current IFDC processes the 4-12 GHz receiver IF range to deliver from each 2SB receiver four 2-4 GHz basebands in 2 polarizations. Doubling the processed bandwidth by simply doubling the number of digitizers would be impractical and doubling the number of quadrants in the correlator room would be impossible. Two approaches are possible to double the bandwidth of the current basebands: either purchase and qualify an analog-to-digital converter (ADC) clocked at or above 8 GHz, or design and fabricate a custom ASIC. The commercial approach is not as simple as it may look because only very few high speed devices provide a large bandwidth and exhibit low power dissipation. The ASIC approach can more easily meet the ALMA system requirements a priori, but the lead time to delivery and full qualification may be long.

In addition, when considering new fast digitizers two related questions should be addressed:



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- Can we digitize the entire 4-12 GHz IF range to improve IFDC reliability and flexibility?
- What are the consequences of increasing the number of bits to enhance system sensitivity?

In the first case either ultra-high speed ADCs to digitize signals up to 12 GHz with a single ADC are required, or, with a multi-rate ADC design, somewhat slower ADCs can be used (Fig. 2, Ref [2]). Our current survey of commercially available fast ADCs shows that there are only 2 commercial devices with maximum sample rates of 26 and 15 GS/s and a bandwidth around 20 GHz. Both products must be qualified at these high speeds and this has never been made at any observatory as far as we know. (We have discarded here interleaved ADCs because of operational complexity with a multi-antenna array such as ALMA.)

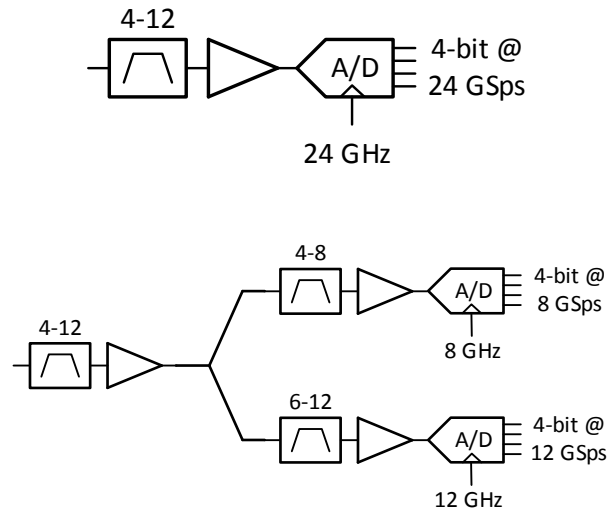


Fig. 2: Ultra-wide band (top) and multi-rate (bottom) sampling concepts (Ref [2])

Higher bit resolution (second bullet above) compared to the current 3 bits would improve the digital efficiency, and hence, ALMA sensitivity. With 8 times more lags provided by the correlator upgrade, 4-bit correlation should become a standard mode which, combined with 4-bit digitization, would nicely improve ALMA sensitivity. We expect to reach 98% efficiency (4-bit digitization and correlation) compared to the current 84% efficiency achieved with 3-bit digitization and 2-bit correlation. However, this performance enhancement is achieved at the cost of more dissipated power in the digitizer module and more information to be transmitted in the DTS (see next Section).



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We are aware of two groups working on fast digitizers and modification of the IFDC in view of new prototypes for the ALMA array. A first group at NRAO, Socorro plans to use the ultra-fast 3-bit ADC from Hittite at 24 GS/s to digitize the 4-12 GHz IF range (Ref [3]). A second group at Laboratoire d'Astrophysique de Bordeaux (LAB), University of Bordeaux, has captured data up to 20 GHz with the Hittite 3-bit device and works now on a multi-rate 4-bit sampling concept (with two clocks at 8 and 12 GHz) to digitize the 4-12 GHz IF range (Ref [2]). In both groups, digital processing is performed in large FPGAs to extract 4 GHz basebands from the 4-12 GHz USB and LSB receiver intermediate frequency bands.

Very high speed new digitizers coupled with large new generation FPGAs extracting signal basebands in a flexible way should improve the flexibility and robustness of the current IFDC. However, two additional considerations must be kept in mind when upgrading the digitizer and the IFDC:

- (a) The impact on the digitizer clock module must be evaluated
- (b) A new analog interface between the Front End IF warm output and the new digitizer must be designed

(a) In order to use the current 4 GHz digitizer clock module, the new digitizer design can simply multiply the 4 GHz clock signal by 6 (for the Hittite ADC) or 2 and 3 (double rate ADC design). It is expected that the current 4 GHz clock signal power is adequate to drive these multipliers. One must also consider the impact of generating a clock frequency higher than 4 GHz on subsample delay tracking which is performed by shifting the phase of the 4 GHz clock module. Phase adjustments to about 1/8 sample provides a minimum loss of signal-to-noise ratio at 4 GHz. This is achieved in practice in the current module with $360^\circ/16$ phase steps. These steps seem acceptable for the x2 and perhaps x3 clock signals, but the loss is higher at the high frequency edge of the baseband in the x6 clock signal case. The fine phase adjustment implemented in the lookup tables of the clock module should be adjusted accordingly.

(b) Replacing the current IFDC will require to develop a new analog interface card between the warm IF delivered by the Front End receivers and the new digitizers. As in the first stage of the current IFDC, this interface card must include signal amplification, gain equalization and power control at the ADC input.

Finally, we recommend regular surveying of commercially-available fast ADCs and to manage contacts with existing companies to identify potentially interesting new market products, despite suitability to radio astronomy may not be guaranteed a priori. The maximum speed and effective number of bits to be expected from projections of existing and state-of-the art commercial ADCs tend to indicate that multi-bit devices clocked at tens of GHz should appear in a near future. However, projections are uncertain and show that power dissipation quickly increases with the conversion rate and the number of bits.



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Recently developed IP cores provide very high speeds but to the prejudice of complex multi-channel interleaving and, moreover, integration in ADC modules will degrade the ADC performance.

3.3 Data Transmitter and Fiber Optic Multiplexer

The current ALMA DTS (see Fig. 3 taken from Ref [4]) needs to be modified to:

- Double the processed bandwidth
- Improve the current digitizer sensitivity (e.g. 4-bit resolution)

The current DTS consists of a data transmitter module (DTX), a fiber optic dense wavelength-division multiplexer (DWDM) which is the main element of the fiber optic DWDM module (FOM) and, at the other end of the fiber cable, a fiber optic amplifier/demultiplexer (FOAD) and a DTS receiver (DRX). The changes needed for the DTX and FOM are discussed here and the FOAD and DRX changes are presented in the next Section.

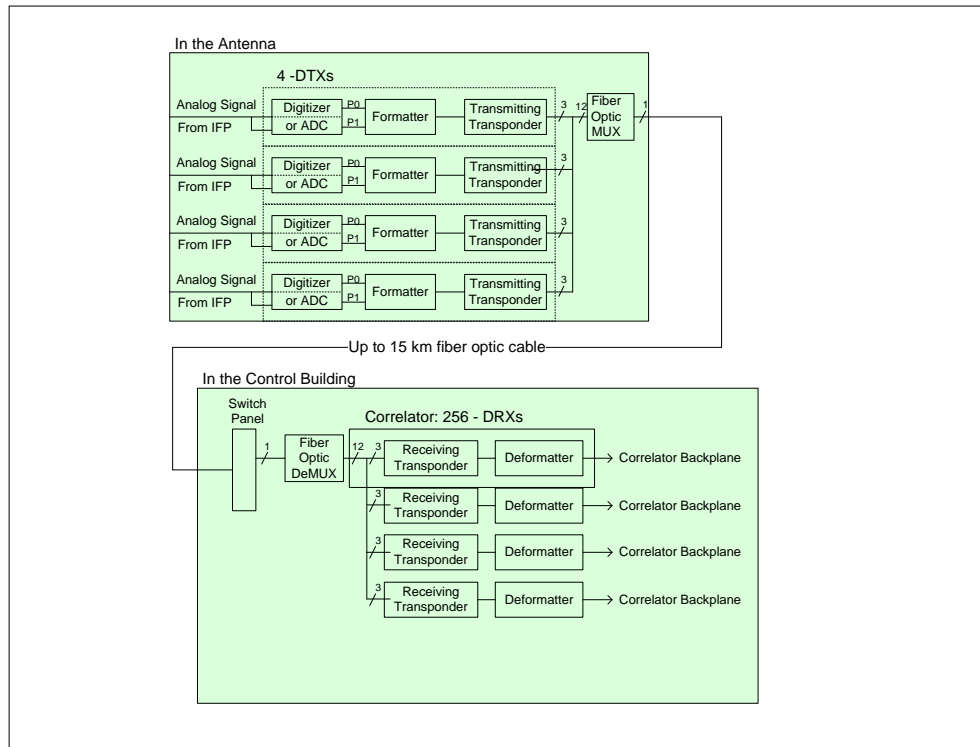


Fig. 3: Overview of the current Data Transmission System (DTS) (taken from Ref [4])



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New DTX formatter/transmitter module:

- The current DTX includes the digitizer assembly whose signal is passed to a formatter board with transponders (one transponder per bit and for 2 polarizations). Each DTX outputs 3 x 10 Gb/s optical signals and there are 4 DTXs per antenna for the 4 baseband pairs (see upper part of Fig. 3 and Fig. 4).

- The new digitizer design requires to replace the current formatter/transponder board by a new board. If we digitize 8 GHz bandwidth per sideband in 2 polarizations, consider 4 bits per sample and include bit encoding, we need to transmit 320 Gb/s from each antenna. This corresponds to 32 x 10 Gb/s data lines instead of the current 12 data lines per antenna shown in Figs. 3 and 4. One large FPGA can capture the digitized signals (see some details below) from 2 polarizations for each receiver sideband and extract for a given sideband two 4 GHz channels per polarization. Data channelization and processing would then be implemented in 2 large FPGAs, each one processing one receiver sideband in 2 polarizations. Two DTXs per antenna would now be sufficient instead of the current 4, and each new DTX would output 16 data lines (4-bit x 4) corresponding to 16 different wavelengths per polarization pair and sideband. This new hardware arrangement divides by 2 the number of DTX modules and keeps the LRU 'model' for the antenna digital racks.

- The current DTX includes a Monitor/Control and Power Supply card which is mounted in the middle of the module. It is hoped that the power required for the new digitizer and formatter cards will be compatible with the existing power supply (or will need minor upgrade when proposing the new design). However, details of the power cycling needs to be changed.



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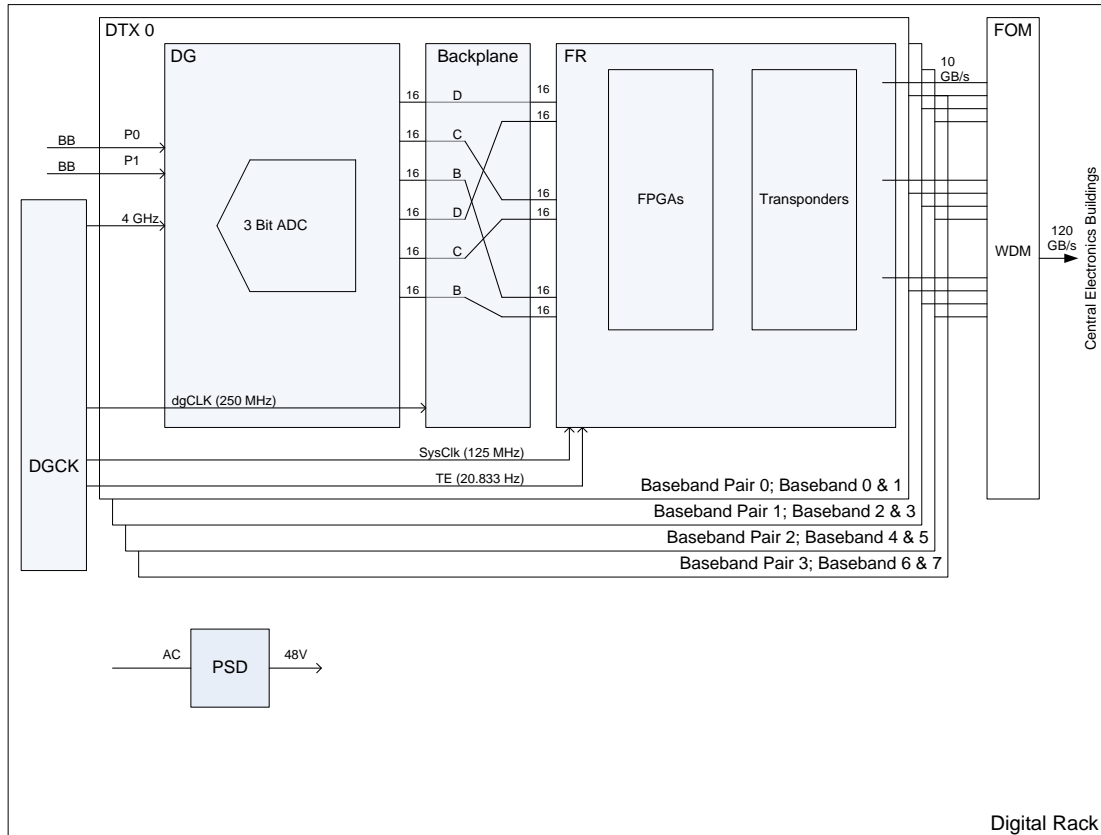


Fig. 4: Current DTX and FOM in antenna digital rack (see Ref [4])

- When designing the new formatter/transmitter card which follows the new digitizer, data capture and clock transmission become major problems because of delays in the transmission lines and because of higher data rates resulting from bandwidth doubling. These problems can be solved with new generation FPGAs using the transceiver technology. The encoding stage to be designed at the data capture level is critical. It must provide a high toggle rate for proper clock recovery and an ‘initialization’ sequence to synchronize the n-bit physical lines from the digitizer. When the data have been unscrambled and processed (e.g. subband extraction) another encoding stage is applied to the data (e.g. 8b10b encoding) before each optical carrier is modulated at 10 Gb/s.

- The LAB group has demonstrated with an Altera device that 3-lane synchronization and good data transmission up to 12 GHz without clock-unlocking is feasible. They propose now (Ref [2]) to study 4-bit data transmission and to implement two firmwares to extract either 2 or 4 GHz basebands for further processing in the current or upgraded TFB cards. A similar new study (Ref [3]), recently started by the NRAO



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group at Socorro, proposes to replace the current 3-bit ADC and IFDC by a 3-bit, 24 GHz clocked ADC and digital IFDC processing to extract 4 GHz basebands. The large FPGAs used in both groups provide optical transceivers for 10 Gb/s links to the existing fiber.

In any case, for easier interface to the ALMA system, the new formatter card design should also provide the characteristics embedded in the current DTX, that is:

- De-Walshing on the sign bit, each bit being separately identified
- Incorporate test patterns

- We note another potential simplification with respect to the current design. One may not need to send the digitized signals to the new formatter card through the antenna digital rack backplane if we use FPGA mezzanine card connectors to directly link each digitizer pair outputs to the new formatter card.

New DWDM:

- In the current system, 12 different wavelengths from the 4 DTX units of each antenna are multiplexed in a passive DWDM module to send all digitized signals from each antenna through one fiber of the multi-fiber cable to the correlator room in the technical building. (Fiber multiplexing enables to carry all signals over long distances without needing to trim individual fibers to a given length.) ALMA currently uses 200 GHz channel spacing DWDM technology which can transmit up to 20 channels on a single mode fiber.

- A more recent DWDM technology must be identified to implement the bandwidth upgrade and/or 4-bit digitizers. Several possibilities are available on the market, e.g. 100 GHz channel spacing DWDM with up to 40 channels. This is adequate to accommodate 320 Gb/s from each antenna (x2 bandwidth and 4 bits) carried in 16 x 10 Gb/s links from each new DTX, assuming that we adopt 2 DTXs per antenna. Even if only 3 bits per sample are transmitted, 24 x 10 Gb/s channels are needed with twice more bandwidth, so that the current DWDM in the FOM module must also be changed. We thus need to use either 32 or 24 different wavelengths for the upgrade with 4- or 3-bit digitizers, respectively.

- Another design approach consists in using the FPGA optical transceivers to directly transmit the 10 Gb/s signals to an active DWDM system that includes compact optical transceivers. This would simplify the DTX card design (same approach is possible for the DRX, see next Section). There should be enough room left in the antenna Back-End digital rack to replace the current passive DWDM system by a new, recent technology active DWDM.



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3.4 Fiber Optic Demultiplexer (FOAD) and new DRX

We briefly describe here the changes required in the FOAD-DWDM racks (in patch panel room) and in the DRX cards (in correlator room). The encoded data are transmitted from the antennas to the patch panel room in the AOS technical building and there is one single fiber assigned to each antenna. All 64 antenna fibers coming out from the main patch panel racks are sent to 64 FOAD modules (see e.g. Ref [4]).

FOAD-DWDM and interface fibers:

- In the current system, each FOAD receives one fiber, demuxes the data by wavelength in one passive DWDM identical to the antenna passive DWDM and outputs 12 fibers. (Each of these fibers carries one of the 12 wavelengths sent from the 4 antenna DTXs.) The DWDM output fibers (we call them here interface fibers) are routed by groups of 3 wavelengths to the correlator room, each group being assigned to one DRX card through openings in the Station rack backplane of the correlator. Each DRX card thus receives data from a single antenna in a single baseband pair and there are four DRX cards per Station rack bin of the correlator to process all 4 baseband pairs. (4 x 64 DRX cards are distributed in 4 x 4 Station racks of the full 4 quadrants of the correlator system.)

- Doubling the processed bandwidth has two consequences: (a) The FOAD-DWDMs must be changed. (b) The number of interface fibers needs to be increased if one keeps 10 Gb/s links.

New DWDM and interface fibers:

- Like for the other end of the antenna fiber a new passive DWDM must be identified to accommodate the 32 or 24 wavelengths sent from each antenna (4- or 3-bit case). As mentioned earlier, an alternative design consists in selecting an active DWDM that incorporates the optical transponders thus simplifying the DRX card design (see below).

- The interface fiber layout from the DWDM racks to the correlator room must also be modified with wider bandwidths. There are 768 interface fibers in the current system and we would need 1536 (24 x 64) or 2048 (32 x 64) fibers for the 3- or 4-bit case. This is a total of 6 or 8 fibers at 10 Gb/s to be connected to each DRX card (to be compared to 3 fibers with the current DRX). This could be manageable with always more compact optical adaptors from the market and with a simplified DRX card design (without the optical transponders).

The fiber optic transceiver technology evolves rapidly (e.g. SFP28) and 20 or 40 Gb/s (or more) fiber optic transmission combined with recent DWDM systems could be considered for the ALMA upgrade.



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New DRX implementation:

- The current DRX card demuxes the 10 Gb/s data to lower the data rate (down to 62.5 MHz per polarization channel), aligns the bits and outputs 3-bit x 32 samples at 125 MHz for each antenna and each polarizations. (Two polarizations are processed in one DRX and 125 MHz output signals sent to 2 different TFB cards.) Bit alignment is needed because the 3 bits of a given baseband are not transmitted at the same wavelength and the delay varies with wavelength due to fiber dispersion. To align the bit channels ALMA uses a 'meta-frame bit' and other protocol bits (see data signaling protocol in Ref [5]) inserted at the DTX and recovered in the DRX. (The data captured by the DRX are asynchronous with respect to the system clock.) Signal losses may occur during ALMA operations for various reasons so that the current DRX must also be able to repeat measurements of the transmission delay. Transmission time is known by estimating the time it takes to detect the 'meta-frame bit' at the DRX and comparing to the correlator 'Timing Event'. (Signal transmission takes about 20 microseconds for a 16 km long fiber and ALMA uses 16 ns long counts for this measurement.)

- With more wavelengths than the current 12, a new DRX with the required optical receivers needs to be designed. If transponders are incorporated in the new DWDM all optical receivers will be directly connected to the FPGA transceivers. The main functions described above for the current DRX and test patterns generation must be implemented in the new DRX. This includes:

- Bit alignment following fiber transmission
- Delay time measurement
- Test patterns provided for correlator testing

Because of the new bit encoding associated with the new fast digitizer, the current ALMA bit frame organization may be changed and bit decoding will be adapted to the new scheme implemented in the new DTX formatter.

- Different card implementations of the DRX functions are possible with the current infrastructure. The favored option consists in designing a single DRX/TFB card that incorporates all of the new DRX and TFB functions (and assembling in a single card two TFBs for two polarizations). This card would be plugged into the existing DRX slot and could be connected to the Station Card (SC) shown in Fig. 1 with flexible and controlled cables to avoid transmitting 250 MHz data through the Station electronics backplane. This new card configuration would also free the TFB card space in the Station racks of the correlator.

We stress that adopting an active WDM solution with no transponders in the DRX would benefit to the new DRX/TFB design.



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3.5 New DRX/TFB Card

In the current system each DRX outputs 3 bits times 32 samples at 125 MHz for each polarization of a given baseband pair. These two polarizations are processed in two separate TFB cards and each TFB card extracts from the digitized 2 GHz baseband (4 GS/s) 32 frequency-mobile subbands of 62.5 MHz. This filtering design is implemented in 16 small FPGAs per TFB card and is optimized in terms of power dissipation and resources usage ((Ref [6])). Upgrading the current firmware in these old generation FPGAs is possible but we would not benefit from the most recent large FPGA resources allowing us to drastically simplify the current 4 x 4 FPGA matrix design and to easily double the clock frequency (as required for bandwidth doubling).

A recent study was completed by the LAB group in Bordeaux to show that a single large FPGA is adequate to extract 32 mobile 125 MHz wide subbands from an original 4 GHz baseband. The results are based on a DSP mathematical model and available FPGA resources (Ref [7]). This preliminary study also shows that a single FPGA performing all TFB functions would significantly lower the PCB and FPGA costs.

In the current system two TFB cards process two polarizations from a single DRX. However, a small number of new generation FPGAs would now allow us to implement all functions of a single DRX card and of two TFB cards in a single new DRX/TFB card. Ultimately, the new DRX/TFB card, delivers 2 bits x 32 parallel signals at 250 MHz for each polarization to one correlator Station card. As mentioned in the previous Section, direct 250 MHz card-to-card links with ‘flex’ cables to the Station Card could be proposed while the new DRX/TFB and SC cards would be plugged into the card slots of the existing infrastructure.

4 Summary of Recommended Hardware Changes

We have assumed that improved Front-End receivers will soon provide more bandwidth to match the proposed correlator upgrade and we have briefly described the hardware changes that are required by this upgrade. We summarize below what could be recommended as of today.

General recommendations or remarks

- New modules or cards required to accommodate the correlator upgrade should use as much as possible the existing infrastructure, including supplied power supply voltages.
- Coordination between groups developing new digitizers would be desirable in parallel with surveying commercially-available new products.



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- Coordinated upgrade of new designs required for Back-End DTX and DRX cards and Correlator Station and Baseline electronics cards should continue.
- Simultaneous testing of all subsystem changes versus separate subsystem changes would deserve an investigation in terms of overall upgrade efficiency.

Specific recommendations

- Digitize at least 4 GHz baseband or, preferably, the full IF range.
- 4-bit digitization would be desirable to improve ALMA sensitivity.
- Consider finer phase adjustment in clock module for subsample tracking to minimize SNR losses with faster digitizers.
- Design robust new analog interface between new receiver warm IF output and new digitizers input for signal amplification and equalization and power control.
- Design new DTX formatter/transmitter card with new generation FPGAs allowing flexible extraction of 4 GHz basebands, or other basebands, from new fast digitizers.
- Consider DTX baseband channelization leading to twice less DTXs per antenna.
- Identify mature and cheap DWDM technology to improve the number of wavelength channels.
- Consider active DWDM systems to get rid of transponders in DTX and DRX cards.
- Implementing new DRX and new TFB functions in a single card would be desirable.
- Investigate best interface fiber layout between FOAD racks and correlator room for more than the current 12 fibers per antenna.

5 References

Ref [1] Escoffier, R., Webber, J., Baudry, A. 2005, “64-Antenna Correlator Specifications and Requirements” ALMA-60.00.00.00-001-B-SPE

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