North American ALMA Science Center

Development Upgrades of the Atacama Large Millimeter/submillimeter Array (ALMA)

Project Proposal

A Significant Upgrade to the ALMA 64-Antennna Correlator

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ABSTRACT

The objective of the "ALMA2" upgrade to the 64-antenna ALMA correlator is to double the processed bandwidth of the ALMA system and to increase the spectral resolution of the correlator by a factor of eight. A byproduct of this upgrade will be to increase the observational efficiency significantly in some cases. This upgrade is aligned with the ASAC recommendations for ALMA 2030 primarily by providing larger bandwidth. Doubling the bandwidth would bring "scientifically significant increases in observation speed"[1] allowing the correlation of the entire 4 to 12 GHz IF band. It is aligned with the goal of longer baselines by providing memory to accommodate baselines of 300 km. Moreover, the increase in spectral resolution allows for the use of the more sensitive 4-bit-by-4-bit correlation with greater spectral resolution than the current 2-bit-by-2-bit correlation allows. Wider spectral windows may be imaged due to the increased spectral grasp. Spectral resolution is improved to 1 KHz. New design features will provide limited ability to conduct observations with time resolution 16 times better than the present correlator. In short, it makes ALMA substantially more efficient, at all bands, for a modest cost.

The upgrade philosophy is to implement the changes with minimal cost, minimal risk, and minimal disruption to the ALMA system and with as much of the current ALMA correlator infrastructure, software and firmware retained as possible.

Doubling the bandwidth and increasing the resolution of the correlator requires the development of a new custom correlator IC roughly 32 times more complex than current ALMA1 ASIC. Fortunately, the increase in the capacity of integrated circuit technology (Moore's Law) since the design of the original correlator makes this increase possible. It also requires the replacement of most of the cards in the signal path, nearly 2000 all told.

The upgrade system will continue to support the phased ALMA interface for Very Long Baseline Inteferometry (VLBI).

Requests to include "High Time Resolution" (HTR) features in the correlator have recently been made. However, there has been insufficient time to develop detailed requirements and designs. This can be done during 2017. As a place-holder, funding for "hooks" for HTR have been put into place in the upgrade design for interfacing to a future transient machine. This interface will allow streaming of raw lag integrations to the external transient system to provide time resolution of 1 msec in FDM and 1/32 msec in TDM.

The project strategy will be to develop a minimum cost approach in hardware and labor for implementation of the upgrade. Existing hardware and infrastructure, where possible, will be retained

[1] 1 A ROAD MAP FOR DEVELOPING ALMA, ASAC, Recommendations for ALMA 2030, Bolatto et. al.

unmodified. Control software will require only minor modifications. Circuit cards will be replaced; cables will be added; data acquisition software will be upgraded. Please see details in Appendix B.

It is anticipated that this project will proceed in parallel with a project at Universite de Bordeaux to upgrade the digitizers, some parts of the Data Transmission System (DTS) and the digital filters. Upgrades to other systems, but not as major, will be required to take advantage of this upgrade. The upgrade could be done in two stages (if this were considered useful); first, the resolution increase could be made, followed later by the bandwidth increase. This strategy would allow most of the correlator modifications to be made and verified using existing ALMA infrastructure (existing digitizers, DTS, etc.). Later, as upgrades to the ALMA system have been fully verified and become operational, the bandwidth upgrade could be brought on-line. The disadvantages of the latter approach include more telescope downtime, more software effort and more commissioning time.

The upgrade's testing strategy is designed to minimize risk and downtime to the ALMA system. First printed circuit boards will be individually tested in custom test fixtures. Next, system tests will be conducted in Charlottesville on a system, dubbed "the fifth quadrant", which closely mimics a full quadrant of the correlator. This test fixture will allow testing of interfaces between cards, burn-in of cards and the development and testing of software which will closely match the software that will be deployed at the AOS. Next, the system will be tested on a "fifth quadrant" resident at the OSF. This will add the capability of testing the upgrade with the entire system including antennas, receivers, samplers, etc. Given that there will be rigorous testing prior to installation at the AOS and that the upgrade requires primarily the replacement of existing cards and computers, the installation of the new hardware as well as PAS-level testing could be accomplished with less than a month of down-time. Please see Appendix E for additional detail. Since control software changes will be minimal, we expect that commissioning will be uneventful. However, the impact on operations beyond the PAS level must be estimated by ALMA.

In addition to the upgraded correlator at the AOS, this project would provide another tangible benefit to ALMA: an upgraded test environment. The project, as currently budgeted, will provide hardware to upgrade an existing test facility dubbed the "fifth quadrant" at the OSF and provide a second "fifth quadrant" in Charlottesville. New, simulated data sources, called DTS Simulators, will be designed for this test system. They will provide a lot of flexibility for testing all the correlator modes in Charlottesville and additional test options at the OSF. These resources provide an excellent risk mitigation strategy for this project. The fifth quadrant in Charlottesville can be used for initial system tests with artificial data sources. The fifth quadrant at the OSF can then be used to test the response of the system with one or more telescopes pointed at the sky. This approach minimizes the risk of unforeseen subtle problems at the AOS. The Charlottesville fifth quadrant should also prove useful after the AOS upgrade in support of commissioning and software development, minimizing response time to any issues that are discovered.

This proposed correlator system enhancement would serve to provide ALMA with an easy, fast, and inexpensive path to enhanced performance, with the expectation of the possible availability of a more versatile software correlator in 10 to 15 years.

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1.0 Co-Investigator(s) and Collaborating Institution(s)

Table 1.0: Co-Investigator(s) and Collaborating Institution(s).

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2.0 Subcontractors

2.1 Company/Institution: University of Virginia

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Subcontracted parts and/or services: Dr. Mircea Stan, University of Virginia, will provide expert guidance in the selection of the vendor for the most expensive item in the upgrade, the Application Specific Integrated Circuit (ASIC). As can be seen from his CV in Appendix D, he is an expert in this field.

Note: ASIC design and production and PCB design/manufacture/assembly will be done by outside companies. However, these can only be determined once money for the project is received, and will be determined by competitive bidding.

3.0 Science Case

Science Benefits ALMA science will benefit from an upgraded correlator in several ways:

- ALMA will meet its specification for resolving thermal line widths in cold contracting cores at its lower implemented frequencies; currently this specification is only met at 211 GHz and higher frequencies using uncommissioned 'twice Nyquist' correlator modes.
- In the upgraded correlator proposed here, where the broadest spectral coverage or highest spectral resolution is not needed, 4-bit x 4-bit and double Nyquist modes could be used, providing higher efficiency observations. Use of sensitive 4-bit x 4-bit modes, made more accessible with the upgrade, would cut integration times 12 % (for the full array, the equivalent of an increase of eight antennas in collecting area).
- Band 6, 9 and 10 currently can present more bandwidth to the correlator than it can process, also true of the prototype B2 cartridge under construction at CDL. One goal of the upgraded correlator is to increase the bandwidth processed by the correlator by a factor of two to 16 GHz x 2 polzns. Broader spectral windows also provide additional continuum sensitivity; increasing the depth to which a deep field, for example, might be imaged in a given time. A spectral survey might be undertaken more efficiently owing to the increased bandwidth, as relatively less overhead is needed for calibrations.
- ALMA's instantaneous spectral grasp is increased–for narrow-lined objects which need fine resolution, as wider spectral windows may be imaged.
- High time resolution would be available for measurement of solar events, pulsars or fast transients.

Improved spectral grasp at high spectral resolution Currently, the commissioned correlator modes include eight dual polarization modes, one with coarse frequency resolution in Time Division Mode (TDM; used normally for continuum) and seven in higher frequency resolution Frequency Division Mode (FDM). Each of the FDM modes offers 3840 channels across bandwidths chosen from 1875, 938, 469, 234, 117 or 58.6 MHz total width. The default Hanning weighting then limits spectral resolution to values between 0.03 MHz (0.1 km/s at B3) and 0.976 MHz. (3.3MHz at B3). In the higher resolution of these two modes, appropriate to dense starless cores for instance, the total bandpass at 86 GHz encompasses only 197 km/s, or about 3% of the bandpass. One may have four spectral windows but still only 3% of the total bandpass is covered by the

correlator windows at highest resolution. For sources with relatively narrow spectral lines, such as most galactic sources, a spectral survey with such a limited bandpass would be prohibitively time-consuming, as each spectral setting necessitates additional calibration, a substantial overhead.

With the proposed correlator upgrade, the same set of currently available modes are enhanced: each FDM mode offers 16384 channels with cross polarization products in two baseband channels across bandwidths chosen from 3750, 1875, 938, 469, 234, 117 or 58.6 MHz total width. Therefore, for example, **a spectral survey of an entire 2 GHz bandpass could be made to a resolution of 0.2 km/s with a single frequency setting of a spectral window**. Such a capability would enlarge scientific discovery space, by enlarging the spectral grasp of the instrument, increasing the information delivered to the Principal Investigator and to the archive. Additionally, spectral resolution at ALMA Band 1 (35-51 GHz) would be 0.03 km/s over a 500 km/s wide window. Many energetically low-lying lines occur in this band which would be excited in the cold outer envelope of cores forming stars. This would allow resolution of and comparison of multiple lines. For instance, the J=4-3 line of HC3N at 36 GHz, the hyperfine components of which have been used to measure thermal and non thermal motions within dense cold clouds, and the J=2-1 lines of CH3CN, which has been used to probe cloud temperature. Through intercomparison of line profiles at different energies, the physics and kinematics of the infall envelope may be measured.

Higher spectral resolution One class of interesting narrow lines are those which have self-absorption which indicates infall ("infall asymmetry", Fig. 1 (cf Evans et al. 2015)). ALMA requirement SCI-90.00.00.00-030-00 states 'It shall be possible to configure the corre- lator to achieve sufficient resolution (0.01 km/s) at 100 GHz to resolve thermal line widths', one purpose of which is to resolve the linewidths of cold infalling material.

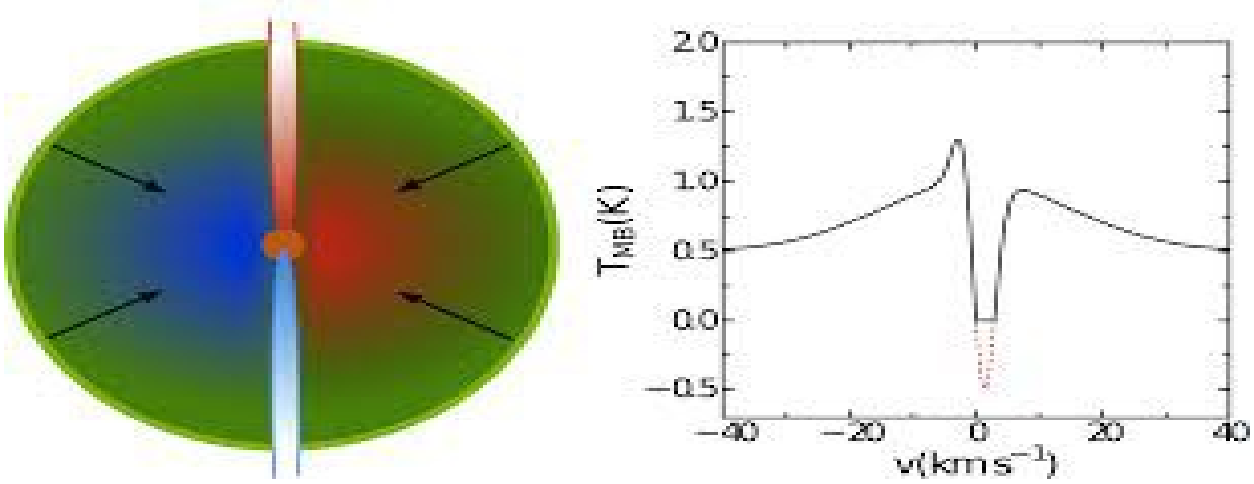


Fig. 1.— Infall Cartoon for First Hydrostatic Core candidates envelope. Material along the line of sight falling onto the protostellar core is redshifted for the observer; that material is cold gas in outer regions of the core. Through resolved observations of various transitions, observations of infall provide a valuable probe of the physics of the outer envelope of the core.

In that case the minimum number of channels across the line needed to model the line properly increases, from perhaps 2 resolution elements = 1 sigma for a simple gaussian line to something like 4 resolution elements = 1 sigma for a line with a dip or a red shoulder. If one applies these criteria to an extreme case (low frequency, heavy molecule, low temperature), then one should consider e.g. the HC3N line at 100 GHz, in a cold, slowly contracting starless core with a central temperature of 8 K. The thermal velocity dispersion would be 0.036 km/s and so the spectral resolution should be about 0.018 km/s to resolve a gaussian line or 0.01 km/s to resolve a self-absorbed gaussian line. ALMA does not currently meet its specification for resolving thermal line widths in cold contracting cores at its lower implemented frequencies at 85 GHz and falls further short for frequencies as low as 35 GHz, for which receivers are now under construction. At 85 GHz with a correlator upgraded as proposed here, the resolution would reach 0.013 km/s, meeting the requirement. Further improvement could be achieved by employing different smoothing functions than the default Hanning smoothing.

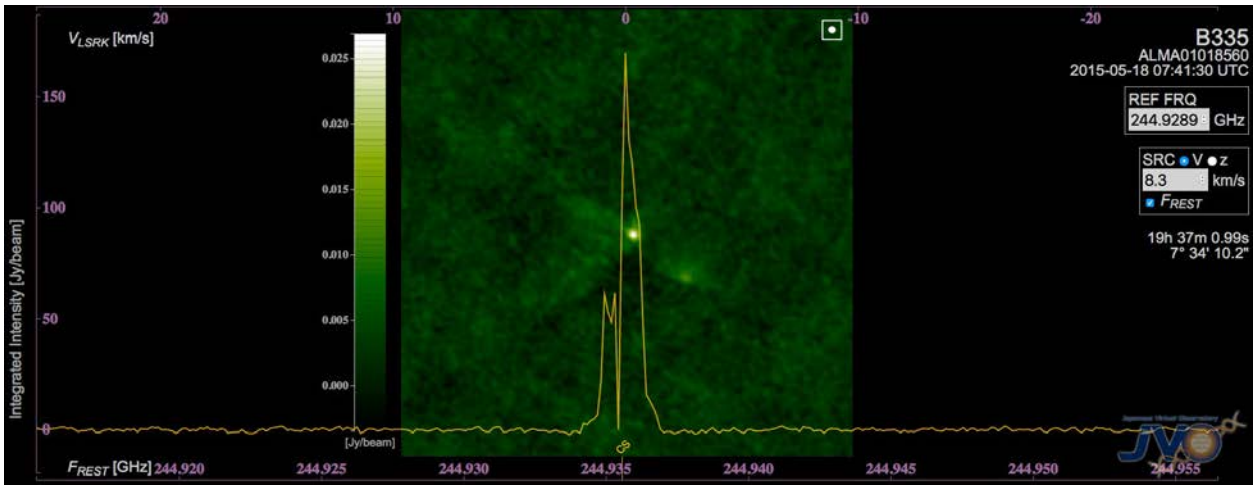


Fig. 2.— ALMA archival data showing the 1.3mm CS J=5-4 line in the envelope of collapsing core B335. Note the apparent complex structure, barely resolved, providing details on the physics and kinematics of the infalling material. Lower excitation lines at lower ALMA frequencies would provide insight into the nature of infall (the axes are reversed in this image, for which frequency lies on the abcissa compared to that in Figure 1). The correlator upgrade would provide the necessary resolution to investigate the kinematics of the cold infalling material.

Increased sensitivity, decreased observing time The efficiency of observing the larger bandwidth may also be improved by the use of the double Nyquist mode. Using 4-bit x 4-bit modes and/or double Nyquist mode (95% efficiency versus 85% including the effect of the 3- bit sampler) is equivalent to adding about 8 antennas to the array or cutting integration times down by 12%. Owing to the details of the way correlator resources are deployed to use these modes, the bandwidth over which they can be used is limited. For example, in a 'continuum' low resolution mode, half the bandwidth would be available (though in 2bit x 2bit modes, the full bandwidth is obtained).

Broader bandwidth, additional spectral grasp The upgraded correlator has twice the spectral grasp of the baseline correlator, that is, 2 sidebands x 8 GHz x 2 polarizations, or 32 GHz as compared to 16 GHz for the baseline correlator. It is matched to the 8 GHz IF bandwidth. For science projects which require maximal spectral coverage, such as spectral surveys or detailed study of line-rich sources, this provides a substantial advantage. In Figure 3, a Herschel/Hexos spectral scan of most of ALMA Band 9 in Orion South is shown. The baseline correlator could cover the 8 GHz window shown in yellow, containing the isotopic CO J=6-5 lines. The upgraded correlator will cover that window in addition to the window shown in blue, containing a number of

weaker lines of $C^{17}O$ and more complex molecules, such as methanol, formaldehyde and CN. To cover both windows with the baseline correlator would require two spectral settings, with substantial calibration overhead. Only one bandpass calibration need be made per spectral setting, rather than several, for the upgraded correlator.

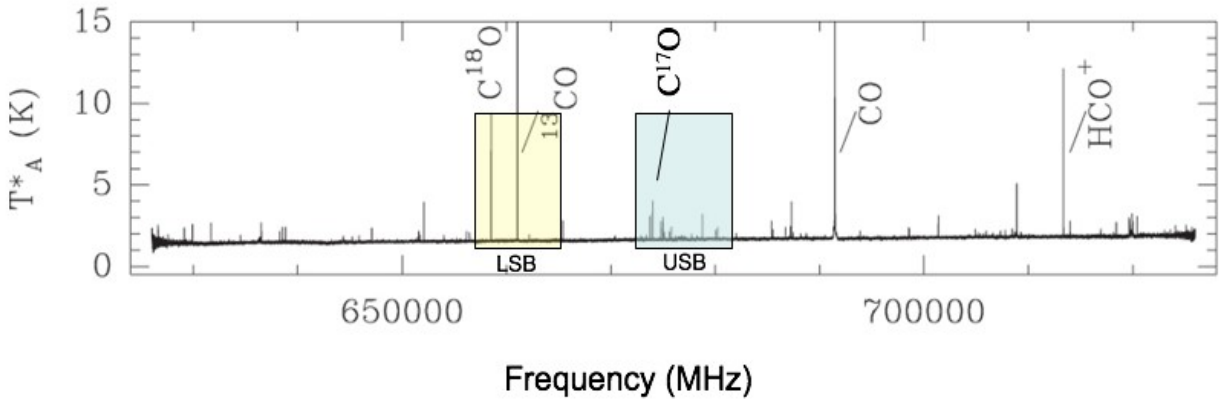
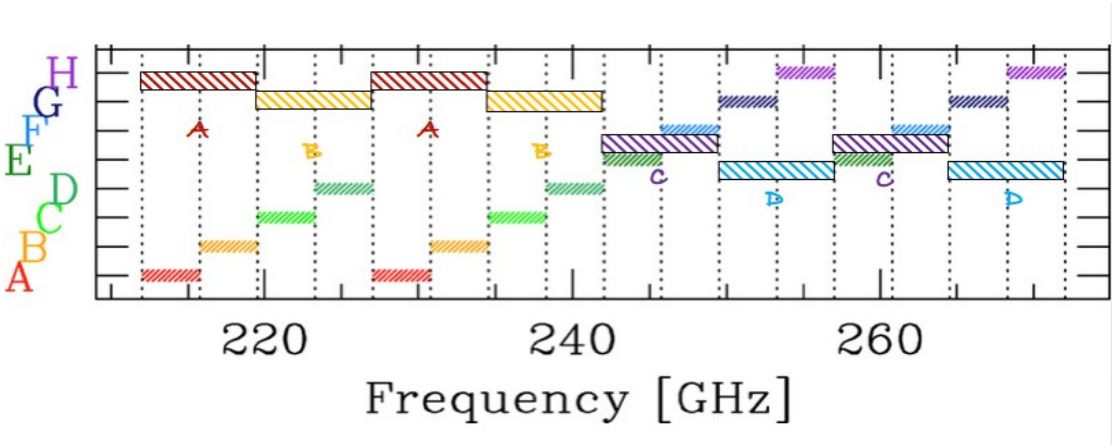


Fig. 3.— A part of the Herschel HEXOS spectral scan in a portion of ALMA Band 9 (611-720 GHz) showing the spectral grasp of the current baseline correrlator (8 GHz x 2 polarizations) compared to that from the upgraded correlator (2 x 8GHz x 2 polarizations). From Analysis of the Herschel/Hexos Spectral Survey Toward Orion South: A Massive Protostellar Envelope with Strong External Irradiation K. Tahani et al. 2016 ApJ 832.

Spectral searches benefit from the increased spectral grasp of the upgraded correlator also. At present three ALMA receivers cover bandwidths which exceed the 2 x (2x2)GHz x 2 polarizations = 16GHz capacity of the baseline correlator: Band 6, with its current 5-10 GHz IF, produces 5GHz x 2 polarizations x 2 sidebands, or 20 GHz. Bands 9 and 10, both DSB receivers with 8 GHz IFs can produce 2x8x2polarizations, of 32 GHz, which matches the processing capability of this upgrade. Studies are under way to upgrade the signal digitization so that increased receiver bandwidths may be conveyed to the correlator. Studies have been published which detail upgrade paths to increased bandwidths for Bands 2 (Bryerton et al 2013), 2+3 (Fuller et al 2016, Beltran et al 2015), Band 3 (Henke et al 2017) and 6 (Kerr et al. 2016). As an example of the improvement in spectral grasp for surveys, the ASPECS survey (Walter et al. 2016) used eight frequency tunings to cover the range of Band 6, each tuning with substantial calibration overhead. The upgraded correlator would only need four frequency settings to cover the same range, in substantially less time. See Fig. 4/



Higher time resolution One could trade temporal resolution for spectral resolution, increasing the number of spectral points per baseband. An uncommissioned mode of the current corrlator provides time resolution of 1 msec for auto-correlation products and 16 msec for cross-correlation products. The addition of RAM to the correlator chip makes it possible to trade time resolution for spectral resolution on auto and cross-products, a new feature which could enable high time resolution spectroscopy of solar events, for instance. A current study (Cordes et al, in progress) should provide ALMA with a capacity for observing pulsars. ALMA's southern hemisphere location makes it ideal for exploration of high dispersion sources near the Galactic Center, such as the recent magnetar outburst, which was observed at frequencies up to 291 GHz (Torne et al 2017). Fast transients provide another interesting possibility; ALMA provided 1.3mm upper limits for instance to the recent identification of FRB121102 (Chatterjee et al 2017). Fig. 4.— A diagram showing the eight Band 6 tunings (Lettered, left) needed to cover the frequencies of the [C II] line at redshifts of 6 to 8 in the ALMA ASPECS spectral scan of the Hubble UltraDeep Field. The four settings needed using the upgraded correlator are shown in the upper bars, noted by script letters.

For the Sun, both impulsive and oscillatory phenomena are expected on sub-second time scales as a result of impulsive energy release in flares. Quasi-periodic oscillations or pulses are seen in hard X-ray and radio emissions, as well as millimeter and submillimeter emission. Kaufmann et al (2009), for example, report peak pulse repetition rates of ~5-10/s in 212 and 405 GHz observations of a powerful X-class flare observed with a time resolution of 5 ms. The origin of the mm/submm pulsations is not understood currently. Their location within a flaring source has not been determined, nor their relationship to OIR and X-ray time variations. The radiative loss time in the chromosphere is of order 2 ms and so a time resolution for correlated data of 1 ms is desirable. Recognizing the trades between time resolution, baselines, and spectral channel are likely necessary, reduced numbers of baselines and channels are acceptable.

The data volume will probably still be extreme. Fast sampling could be implemented as a rotating data buffer or it could be triggered by a total power threshold.

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4.0 Project Scope

The scope of the project includes the design, documentation, construction, board-level test, PAI testing, installation and PAS testing of a system that will provide a factor of two increase in the ALMA 64-Antenna correlator bandwidth and a factor of 8 increase in its spectral resolution. The design includes hardware, firmware and software design. An on-going ALMA correlator study project has already produced detailed designs for most of the hardware

components of the system as well as a design for the required ASIC. Prototyping of a computer interface to handle 8 times the current data rate has also already been accomplished. We expect to prototype FPGA personalities and to do additional ASIC simulations in 2017. Thus, at the beginning of the project, in 2018, the project will be ready for production. In addition to upgrading the correlator, the project will also deliver an upgrade to the proposed "5th Quadrant" test facility at the OSF and a complete similar test facility in Charlottesville.

The project does not include the upgrade of the Tunable Filter Bank cards and the Data Receiver Cards which will be delivered by a parallel project funded by ESO. It also does not include support after PAS, similar to the support provided for the present correlator. This support will be provided by NRAO, but from another funding source.

A detailed specification is included as Appendix A and a more detailed overview of the project is included in Appendix B. A summary of work done to date is included in the list of documents in Appendix C. These documents are available upon request from the PI and may be available from NRAO as the documentation for project PMD-365.

5.0 Project Deliverables

5.1 Hardware

Description	**Number Required**						
Location[1]	**AOS**	**TF, OSF**	**TF, CV**	**TF, BD**	**Spare OSF**	**Spare CV**	**Total**
Printed Circuit Cards							
TFB-to-SC flex board	256	16	16	1	12	2	303
SC	256	16	16	1	12	2	303
SI	128	8	8	1	6	2	153
CI	512	128	128		24	2	794
CC	128	32	32		12	2	206
CC-MEZ	128	32	32		20	4	216
FA	8	2	2		2	1	15

Description	Number Required						
Location[1]	**AOS**	**TF, OSF**	**TF, CV**	**TF, BD**	**Spare OSF**	**Spare CV**	**Total**
DTS-Sim	0	8	8		2	2	20
SCC			4	1		1	6
6U			8	1		1	10
LTA			19			1	20
9U			19			2	21
QCC			0			1	1
Power Control Card			1			1	2
Power Switch Card			1			1	2
CLK		1	6	1	0	1	9
Station Motherboard		1	5	1		1	8
Correlator Motherboard			16			1	17
Spare components							
approximately 5% spare components					4%	1%	
Computer Hardware							
CDP Computers	17	5	5		1	1	29
SFP+ Switches (>8 ports)	4	1	1		1	1	8
Cables							
LVDS (CC to FA)	2048	64	330		40	20	2502
SFP+ LC-to-LC multi-mode	32	4	4		4	4	48
5th quadrant test fixture, CV only							

Description	Number Required						
Location[1]	**AOS**	**TF, OSF**	**TF, CV**	**TF, BD**	**Spare OSF**	**Spare CV**	**Total**
mechanical (racks, bins, etc)			1 lot			0	1
electronics (splitters, switches, etc.)			1				1
motherboards			20			2	22
power supply			3			1	4
power supply, 24V			1			1	2
cables			1				1
Test Fixtures							
CC/LTA + FA		1	1				2
DTS Sim		1	1				2
DRX/TFB - STN (incl one for Bordeaux)		2	1				3

Notes:

[1]: Location indicates the location to which each item will be delivered
AOS: Array Operations Center
TF, OSF: "5th quadrant" test fixture at the ALMA Operations Support Facility
TF, CV: "5th quadrant" test fixture in Charlottesville
TF, BD: Universite de Bordeaux to support delivery and long term maintenance of DRX/TFB card
Spare, OSF: Spare items to be delivered to the ALMA Operations Support Facility
Spare, CV: Spare items to be delivered to Charlottesville in support of the "5th quadrant" test fixture

5.2 Software

- New CDP computer specification, including suitable 10 GbE adapter board.
- CDP Linux kernel configuration to sustain a data rate of 500 MB/sec, or better, inbound and outbound. Minimize UDP datagram dropouts and maximize throughput.
- New correlator modes table implementation.

- Software support for coarse delay updates and residual delay corrections based on a 125ps sample period.
- CCC and CDP functionality compatible with and updated correlator ICD. This includes updated CAN-bus protocols, Ethernet interface between correlator and CDP cluster, data blanking for dropped UDP datagrams.
- System verification in test environment: proper correlator configuration, reception and assembling of lags, CDP pipeline results, sub-arrays verification.
- System integration and validation at AOS.
- Updated Firmware for the correlator's microprocessors
- New FPGA personalities for all new FPGAs.

5.3 Services

- Provisional Acceptance In-house testing 1: to be completed in Charlottesville using a functional replica of the 5th quadrant at the OSF. This will demonstrate the correct functioning of the system with simulated data. A functional 5th Quadrant will remain in Charlottesville as a test bed after this test.
- Provisional Acceptance In-house testing 2: to be completed at the OSF. This will demonstrate the correct functioning of the system with data from a telescope. The main purpose of this test is test the system in as realistic and environment as possible. A functional, upgraded 5th Quadrant will be provided after this test.
- Provisional Acceptance at Site. Installation and testing of the upgrade at the AOS. This is expected to take less than 1 month and leave a system ready for commissioning by ALMA.

5.4 Documents

We intend to follow ALMA documentation requirements. Many documents produced will supersede documents delivered with the original 64-Antenna Correlator. New documents could have new document numbers or simply new version numbers. It is up to ALMA to decide. We will deliver at least the following:

- Monthly "4-Square" Progress Reports
- Specifications
- Hardware design documentation
- Software/firmware design documentation
- Interface Control Documents (ICDs)
- Technical manuals and procedures
- Quality Assurance procedures
- Safety procedures
- Acceptance Test Procedures and Reports
- Closeout Report

6.0 Interfaces to ALMA

The correlator is designed to have minimum impact on ALMA, requiring no changes in physical infrastructure. However, it still has significant impacts on the observatory. The impacts we are aware of are summarized in two reports (hardware and software impacts) that were produced as part of the ALMA correlator study. These are available upon request. An abbreviated summary is included in the table below. As part of the proposal vetting process, ALMA, with its detailed knowledge of all subsystems, is expected to also study impacts; we are available to aid in this effort.

Impacted Element	ALMA Subsystem	Remarks
Receiver	Front-End	Larger instantaneous bandwidth required to take full advantage of the wider correlator bandwidth
Digitization & IFDC	Back-End Digitizer & IFDC	Modifications to IF required to support 4- GHz bandwidth in front of digitizers. Faster digitizers required & digitize full IF range desirable
DTX and fiber optic mux/demux	Data Transmission System	New DTX & DWDM required
DRX Card and TFB Card	Correlator	DRX & TFB functions in a single card desirable
Correlator Control Software	Software	Minimal changes
Correlator Data Processor	Software	Physical interface must change to 10 GbE. Software and hardware upgrade to handle packetization and 8X higher data rate.
TelCal	Software	Must be modified to deal with wider IF, TFB bandwidth and VLBI compatibility
User Interface	Software	Must present new options to the users.

7.0 Period of Performance

Jan 2, 2018 to June 30, 2021.

8.0 Staffing

8.1 Offerer's Staffing

Table 2.0: Labor Estimate.

Please note that there are two possible staffing scenarios and that the table below budgets for the worst case. The first scenario involves the use of Alejandro Saez at his present location in Chile and the hiring of an engineer, "Engineer 2", in Charlottesville approximately six months into the program. The second scenario involves the transfer of Saez to Charlottesville approximately six months into the program and his return to Chile to assist with installation, test and commissioning near the conclusion of the program. The advantages and disadvantages of both approaches are discussed in the following paragraphs.

The first scenario has clear, short-term benefits to ALMA operations. Saez is a key player in day-to-day operation of the observatory. Having him close by minimizes the time-to-repair of several sub-systems. The disadvantages to the upgrade project include poorer communication with Saez due to his remoteness, less time available from Saez due to other duties and the need to hire and train a correlator engineer in Charlottesville.

The second scenario has short-term disadvantages to ALMA operations and significant advantages to the upgrade project in the short term and to ALMA operations in the long term. In the short-term, ALMA would have to primarily rely on the rest of its correlator group for maintenance. This may result in more down time. A small fraction of Saez's time, while he is in Charlottesville, would be available for support of the existing correlator. The upgrade project would clearly benefit from improved availability and communications with Saez. The learning curve for a new hire would be eliminated. Manpower would be saved and the cost of the project would be decreased. ALMA would also, in the long-term, greatly benefit from having Saez heavily involved in the design phase of the project. He was resident in Charlottesville for 3 years during the design of the current correlator and gained intimate knowledge of the design and, importantly, the design tools. We assert that this is in large part responsible for the current high reliability of the correlator and the low mean-time-to-repair. The knowledge Saez gained during his stint in Charlottesville also allowed him to be a key player in the development of several features of the correlator that came along after formal delivery. The sub-array feature is one such example. As a gifted design engineer, Saez is interested in doing more design and less routine maintenance. This project provides a good opportunity for this. Certainly, a worst case scenario, for both operations and the upgrade project, is for him to take his talents elsewhere. The ALMA correlator group may also benefit long term because of the need to solve problems without Saez close by for advice. For these reasons, we believe that the second scenario is significantly better than the first.

JOB TITLE	KEY PERSONNEL	FTE[2]	DURATION (MONTHS)
Principal Investigator	Rich Lacasse	0.75	24
Scientific Lead	Al Wootten	0.01	48
Engineering Lead	Ray Escoffier	0.75	48
Software Lead	Rodrigo Amestica	0.22	48
Research Engineer	John Webber	0.01	48
Senior Engineer	Joe Greenberg	0.2	48
Engineer 1	Alejandro Saez	0.30	48
Engineer 2	New Hire	1.0	42
Software Engineer	Pete Whiteis	0.13	48
Technician 1	TBD	0.75	36
Technician 2	TBD	0.04	36
Machinist	TBD	0.5	1
Project Management	TBD	0.75	48
	TOTALS	**10.66**	**48**

Duration will just be the total length of the project. FTE total is the total FTE allocation over the life of the project.

8.2 External Staffing

Table 3.0: External Staffing and Contact Information.

TITLE	NAME	INSTITUTION	EMAIL	TELEPHONE
Co-Investigator	Mircea Stan	University of Virginia	mircea@virginia.edu	434-924-3503
Vendor Point of Contact	Mircea Stan			
Customer Point of Contact	Mircea Stan			

[2] FTE allocation per person is an average per year based on that resource's anticipated project duration. Total FTE allocation is based on the sum of the FTE allocations anticipated per year.

Co-Investigator	Alain Baudry	Laboratoire d'Astrophysique de Bordeaux, Univ. Bordeaux	alain.baudry@u-bordeaux.fr	
Vendor Point of Contact	Annick Caperan	annick.caperan@u-bordeaux.fr		
Customer Point of Contact	Alain Baudry			

9.0 Cost Breakdown

9.1 Offerer's Cost

Table 4.0: Offerer's Direct Cost Breakdown.

WBS No.	Task Description	Labor ($)	Materials & Services ($)	Travel ($)
1.0	ALMA2 ASIC Dev. And Prod.	$104,613	$3,700,000	$10,000
2.0	Electronics Construction	$182,947	$1,795,019	$2,000
3.0	Test System Construction	$144,428	$771,440	$21,995
4.0	Software Development	$326,526	$203,000	$0.00
5.0	Low-level Firmware and Personalities	$274,754	$0.00	$0.00
6.0	System Integration	$272,293	$30,000	$40,000
7.0	Management	$197,643	$4,000.00	$41,400.00
	SubTotals ($)	**$1,503,204**	**$6,503,459**	**$115,395**
	TOTAL OFFERER'S DIRECT COST ($)			**$8,122,058**

9.2 Collaborating Institution / Subcontractor Cost

Table 5.0: Collaborating Institution/Subcontractor Cost & In-Kind Contribution.

Collaborating Institution / Subcontractor	USD ($)	In-Kind Contribution Value in USD ($)
Mircea Stan	$6,000	
Alain Baudry		$40,000

Ray Escoffier		$394,408
TOTAL COST ($)	**$6,000**	
TOTAL VALUE of IN-KIND CONTRIBUTIONS ($)		**$434,408**

9.3 Total Project Cost

Table 6.0: Total Project Cost.

PROJECT COST ELEMENTS	**USD ($)**
Total Offerer's Direct Cost (Table 4.0) PARTS AND LABOR AND TRAVEL	$8,122,058
Collaborating Institution / Contractor Total Cost (Table 5.0)	$6,000
Project Contingency (requires a supporting Risk Mitigation Plan, Table 9.0)	$1,219,208
Indirect Costs	$1,568,720
TOTAL PROJECT COST ($)	**$10,915,986**

9.4 Cost Distribution (Cash Flow)

Table 7.0: Project Cost Distribution.

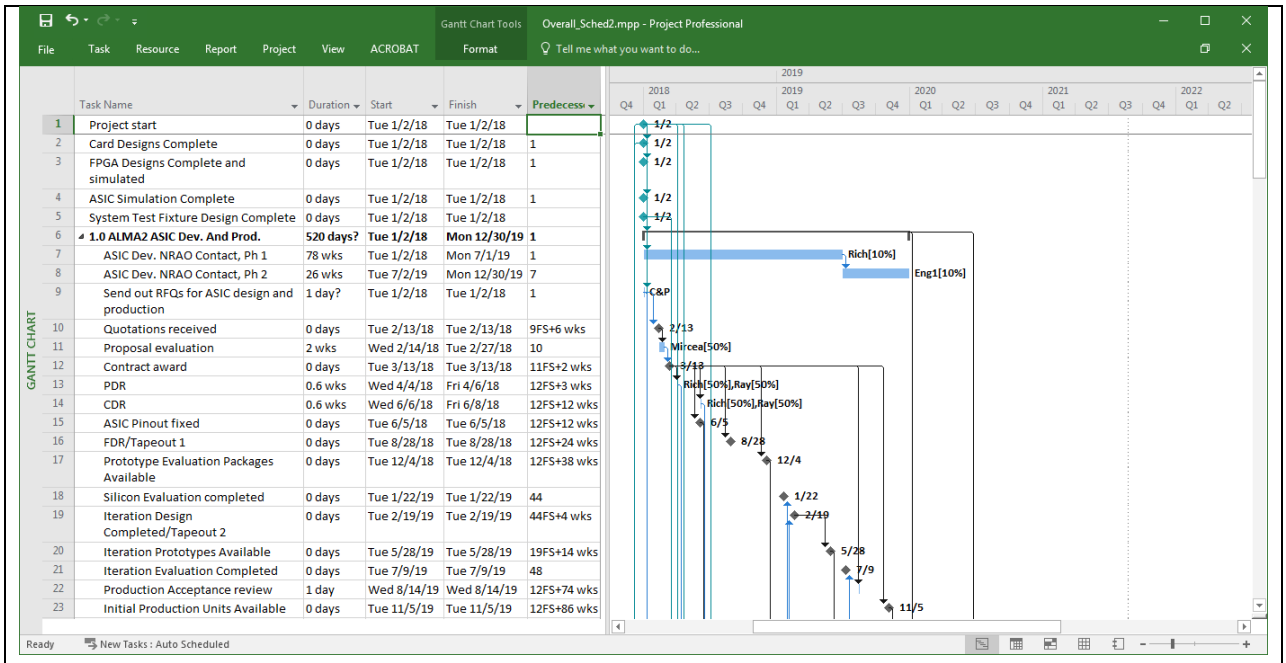
FY2018 COST ($)	**FY2019 COST ($)**	**FY2020 COST ($)**	**FY2021 COST ($)**	**TOTAL COST ($)**
$5,709,457	**$3,606,272**	**$1,063,363**	**$536,894**	**$10,915,986**

9.5 Total Project Value

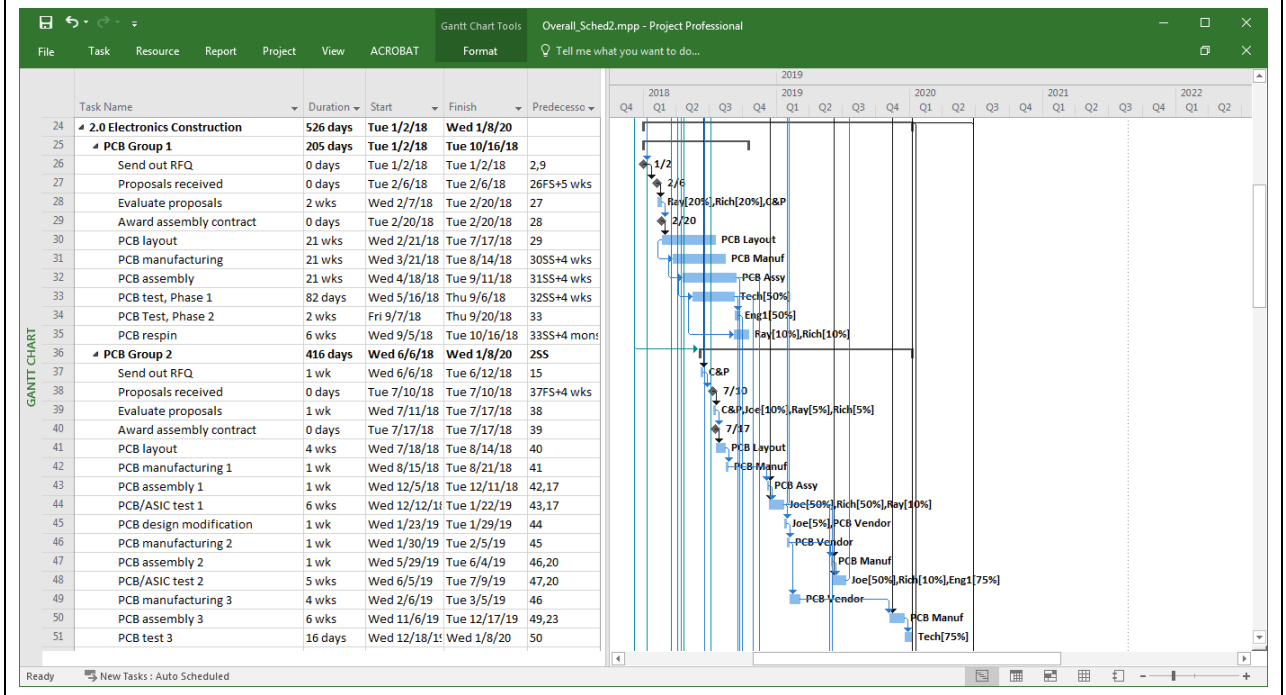
Table 8.0: Total Project Value.

PROJECT ELEMENTS	**USD ($)**
Total Offerer's Cost (Table 4.0)	**$10,915,986**
Collaborating Institution / Contractor Total In-Kind Contributions (Table 5.0)	**$434,408**
TOTAL PROJECT VALUE ($)	**$11,350,394**

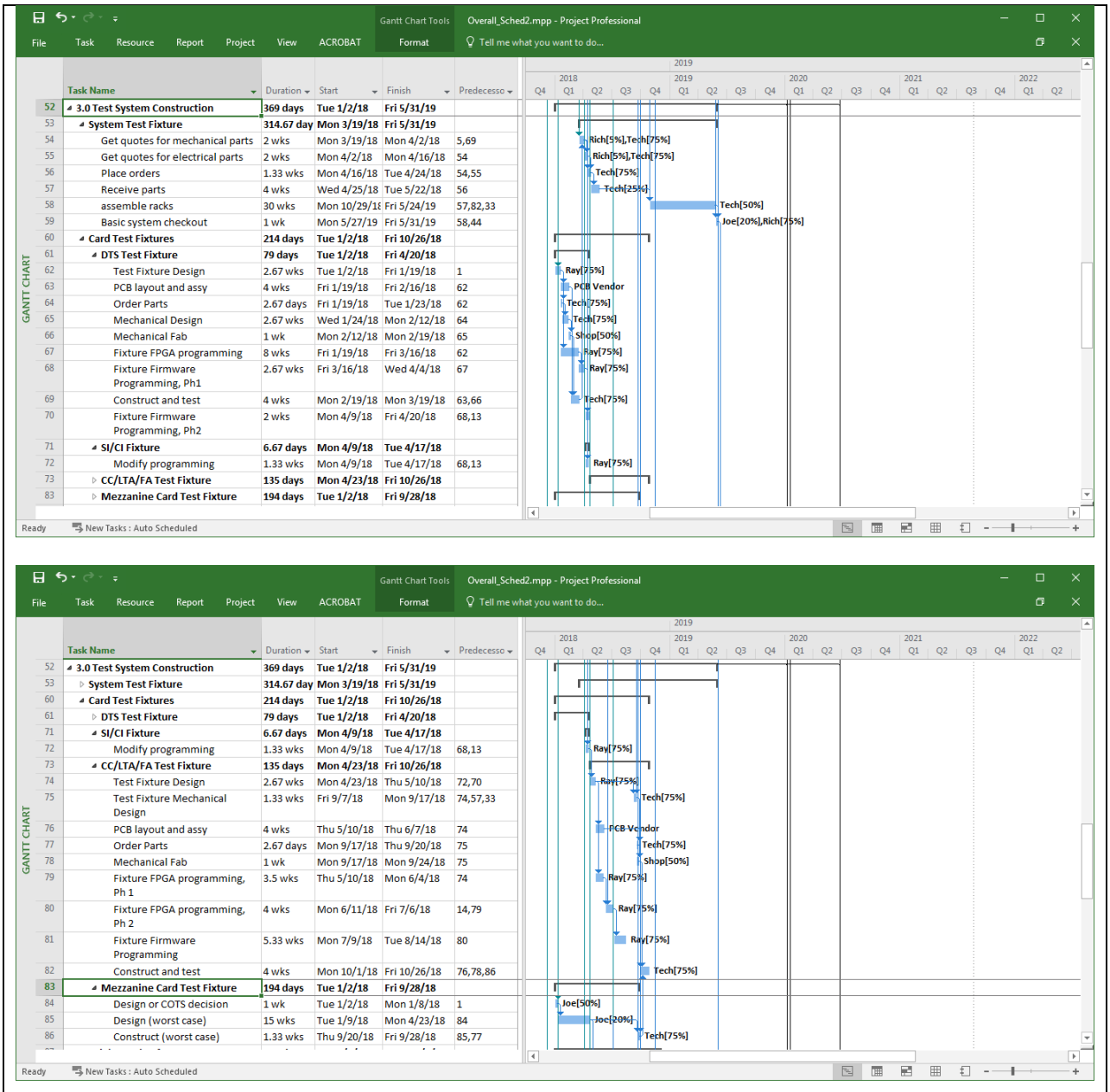
10.0 Project Schedule



	Task Name	Duration	Start	Finish	Predecesso
1	Project start	0 days	Tue 1/2/18	Tue 1/2/18	
2	Card Designs Complete	0 days	Tue 1/2/18	Tue 1/2/18	1
3	FPGA Designs Complete and simulated	0 days	Tue 1/2/18	Tue 1/2/18	1
4	ASIC Simulation Complete	0 days	Tue 1/2/18	Tue 1/2/18	1
5	System Test Fixture Design Complete	0 days	Tue 1/2/18	Tue 1/2/18	
6	**1.0 ALMA2 ASIC Dev. And Prod.**	**520 days?**	**Tue 1/2/18**	**Mon 12/30/19**	**1**
7	ASIC Dev. NRAO Contact, Ph 1	78 wks	Tue 1/2/18	Mon 7/1/19	1
8	ASIC Dev. NRAO Contact, Ph 2	26 wks	Tue 7/2/19	Mon 12/30/19	7
9	Send out RFQs for ASIC design and production	1 day?	Tue 1/2/18	Tue 1/2/18	1
10	Quotations received	0 days	Tue 2/13/18	Tue 2/13/18	9FS+6 wks
11	Proposal evaluation	2 wks	Wed 2/14/18	Tue 2/27/18	10
12	Contract award	0 days	Tue 3/13/18	Tue 3/13/18	11FS+2 wks
13	PDR	0.6 wks	Wed 4/4/18	Fri 4/6/18	12FS+3 wks
14	CDR	0.6 wks	Wed 6/6/18	Fri 6/8/18	12FS+12 wks
15	ASIC Pinout fixed	0 days	Tue 6/5/18	Tue 6/5/18	12FS+12 wks
16	FDR/Tapeout 1	0 days	Tue 8/28/18	Tue 8/28/18	12FS+24 wks
17	Prototype Evaluation Packages Available	0 days	Tue 12/4/18	Tue 12/4/18	12FS+38 wks
18	Silicon Evaluation completed	0 days	Tue 1/22/19	Tue 1/22/19	44
19	Iteration Design Completed/Tapeout 2	0 days	Tue 2/19/19	Tue 2/19/19	44FS+4 wks
20	Iteration Prototypes Available	0 days	Tue 5/28/19	Tue 5/28/19	19FS+14 wks
21	Iteration Evaluation Completed	0 days	Tue 7/9/19	Tue 7/9/19	48
22	Production Acceptance review	1 day	Wed 8/14/19	Wed 8/14/19	12FS+74 wks
23	Initial Production Units Available	0 days	Tue 11/5/19	Tue 11/5/19	12FS+86 wks



	Task Name	Duration	Start	Finish	Predecesso
24	**2.0 Electronics Construction**	**526 days**	**Tue 1/2/18**	**Wed 1/8/20**	
25	**PCB Group 1**	**205 days**	**Tue 1/2/18**	**Tue 10/16/18**	
26	Send out RFQ	0 days	Tue 1/2/18	Tue 1/2/18	2,9
27	Proposals received	0 days	Tue 2/6/18	Tue 2/6/18	26FS+5 wks
28	Evaluate proposals	2 wks	Wed 2/7/18	Tue 2/20/18	27
29	Award assembly contract	0 days	Tue 2/20/18	Tue 2/20/18	28
30	PCB layout	21 wks	Wed 2/21/18	Tue 7/17/18	29
31	PCB manufacturing	21 wks	Wed 3/21/18	Tue 8/14/18	30SS+4 wks
32	PCB assembly	21 wks	Wed 4/18/18	Tue 9/11/18	31SS+4 wks
33	PCB test, Phase 1	82 days	Wed 5/16/18	Thu 9/6/18	32SS+4 wks
34	PCB Test, Phase 2	2 wks	Fri 9/7/18	Thu 9/20/18	33
35	PCB respin	6 wks	Wed 9/5/18	Tue 10/16/18	33SS+4 mons
36	**PCB Group 2**	**416 days**	**Wed 6/6/18**	**Wed 1/8/20**	**2SS**
37	Send out RFQ	1 wk	Wed 6/6/18	Tue 6/12/18	15
38	Proposals received	0 days	Tue 7/10/18	Tue 7/10/18	37FS+4 wks
39	Evaluate proposals	1 wk	Wed 7/11/18	Tue 7/17/18	38
40	Award assembly contract	0 days	Tue 7/17/18	Tue 7/17/18	39
41	PCB layout	4 wks	Wed 7/18/18	Tue 8/14/18	40
42	PCB manufacturing 1	1 wk	Wed 8/15/18	Tue 8/21/18	41
43	PCB assembly 1	1 wk	Wed 12/5/18	Tue 12/11/18	42,17
44	PCB/ASIC test 1	6 wks	Wed 12/12/1	Tue 1/22/19	43,17
45	PCB design modification	1 wk	Wed 1/23/19	Tue 1/29/19	44
46	PCB manufacturing 2	1 wk	Wed 1/30/19	Tue 2/5/19	45
47	PCB assembly 2	1 wk	Wed 5/29/19	Tue 6/4/19	46,20
48	PCB/ASIC test 2	5 wks	Wed 6/5/19	Tue 7/9/19	47,20
49	PCB manufacturing 3	4 wks	Wed 2/6/19	Tue 3/5/19	46
50	PCB assembly 3	6 wks	Wed 11/6/19	Tue 12/17/19	49,23
51	PCB test 3	16 days	Wed 12/18/1	Wed 1/8/20	50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Overall_Sched2.mpp - Project Professional
File Task Resource Report Project View ACROBAT Format
Tell me what you want to do...
GANTT CHART
Task Name Duration Start Finish Predecesso
52 3.0 Test System Construction 369 days Tue 1/2/18 Fri 5/31/19
53 System Test Fixture 314.67 day Mon 3/19/18 Fri 5/31/19
54 Get quotes for mechanical parts 2 wks Mon 3/19/18 Mon 4/2/18 5,69
55 Get quotes for electrical parts 2 wks Mon 4/2/18 Mon 4/16/18 54
56 Place orders 1.33 wks Mon 4/16/18 Tue 4/24/18 54,55
57 Receive parts 4 wks Wed 4/25/18 Tue 5/22/18 56
58 assemble racks 30 wks Mon 10/29/18 Fri 5/24/19 57,82,33
59 Basic system checkout 1 wk Mon 5/27/19 Fri 5/31/19 58,44
60 Card Test Fixtures 214 days Tue 1/2/18 Fri 10/26/18
61 DTS Test Fixture 79 days Tue 1/2/18 Fri 4/20/18
62 Test Fixture Design 2.67 wks Tue 1/2/18 Fri 1/19/18 1
63 PCB layout and assy 4 wks Fri 1/19/18 Fri 2/16/18 62
64 Order Parts 2.67 days Fri 1/19/18 Tue 1/23/18 62
65 Mechanical Design 2.67 wks Wed 1/24/18 Mon 2/12/18 64
66 Mechanical Fab 1 wk Mon 2/12/18 Mon 2/19/18 65
67 Fixture FPGA programming 8 wks Fri 1/19/18 Fri 3/16/18 62
68 Fixture Firmware Programming, Ph1 2.67 wks Fri 3/16/18 Wed 4/4/18 67
69 Construct and test 4 wks Mon 2/19/18 Mon 3/19/18 63,66
70 Fixture Firmware Programming, Ph2 2 wks Mon 4/9/18 Fri 4/20/18 68,13
71 SI/CI Fixture 6.67 days Mon 4/9/18 Tue 4/17/18
72 Modify programming 1.33 wks Mon 4/9/18 Tue 4/17/18 68,13
73 CC/LTA/FA Test Fixture 135 days Mon 4/23/18 Fri 10/26/18
83 Mezzanine Card Test Fixture 194 days Tue 1/2/18 Fri 9/28/18
2019
Q4 Q1 Q2 Q3 Q4 2018 2019 2020 2021 2022
Rich[5%],Tech[75%]
Rich[5%],Tech[75%]
Tech[75%]
Tech[25%]
Tech[50%]
Joe[20%],Rich[75%]
Ray[75%]
PCB Vendor
Tech[75%]
Tech[75%]
Shop[50%]
Ray[75%]
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Ready
New Tasks : Auto Scheduled

Gantt Chart Tools
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File Task Resource Report Project View ACROBAT Format
Tell me what you want to do...
GANTT CHART
Task Name Duration Start Finish Predecesso
52 3.0 Test System Construction 369 days Tue 1/2/18 Fri 5/31/19
53 System Test Fixture 314.67 day Mon 3/19/18 Fri 5/31/19
60 Card Test Fixtures 214 days Tue 1/2/18 Fri 10/26/18
61 DTS Test Fixture 79 days Tue 1/2/18 Fri 4/20/18
71 SI/CI Fixture 6.67 days Mon 4/9/18 Tue 4/17/18
72 Modify programming 1.33 wks Mon 4/9/18 Tue 4/17/18 68,13
73 CC/LTA/FA Test Fixture 135 days Mon 4/23/18 Fri 10/26/18
74 Test Fixture Design 2.67 wks Mon 4/23/18 Thu 5/10/18 72,70
75 Test Fixture Mechanical Design 1.33 wks Fri 9/7/18 Mon 9/17/18 74,57,33
76 PCB layout and assy 4 wks Thu 5/10/18 Thu 6/7/18 74
77 Order Parts 2.67 days Mon 9/17/18 Thu 9/20/18 75
78 Mechanical Fab 1 wk Mon 9/17/18 Mon 9/24/18 75
79 Fixture FPGA programming, Ph 1 3.5 wks Thu 5/10/18 Mon 6/4/18 74
80 Fixture FPGA programming, Ph 2 4 wks Mon 6/11/18 Fri 7/6/18 14,79
81 Fixture Firmware Programming 5.33 wks Mon 7/9/18 Tue 8/14/18 80
82 Construct and test 4 wks Mon 10/1/18 Fri 10/26/18 76,78,86
83 Mezzanine Card Test Fixture 194 days Tue 1/2/18 Fri 9/28/18
84 Design or COTS decision 1 wk Tue 1/2/18 Mon 1/8/18 1
85 Design (worst case) 15 wks Tue 1/9/18 Mon 4/23/18 84
86 Construct (worst case) 1.33 wks Thu 9/20/18 Fri 9/28/18 85,77
2019
Q4 Q1 Q2 Q3 Q4 2018 2019 2020 2021 2022
Ray[75%]
Ray[75%]
Tech[75%]
PCB Vendor
Tech[75%]
Shop[50%]
Ray[75%]
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Tech[75%]
Joe[50%]
Joe[20%]
Tech[75%]
Ready
New Tasks : Auto Scheduled

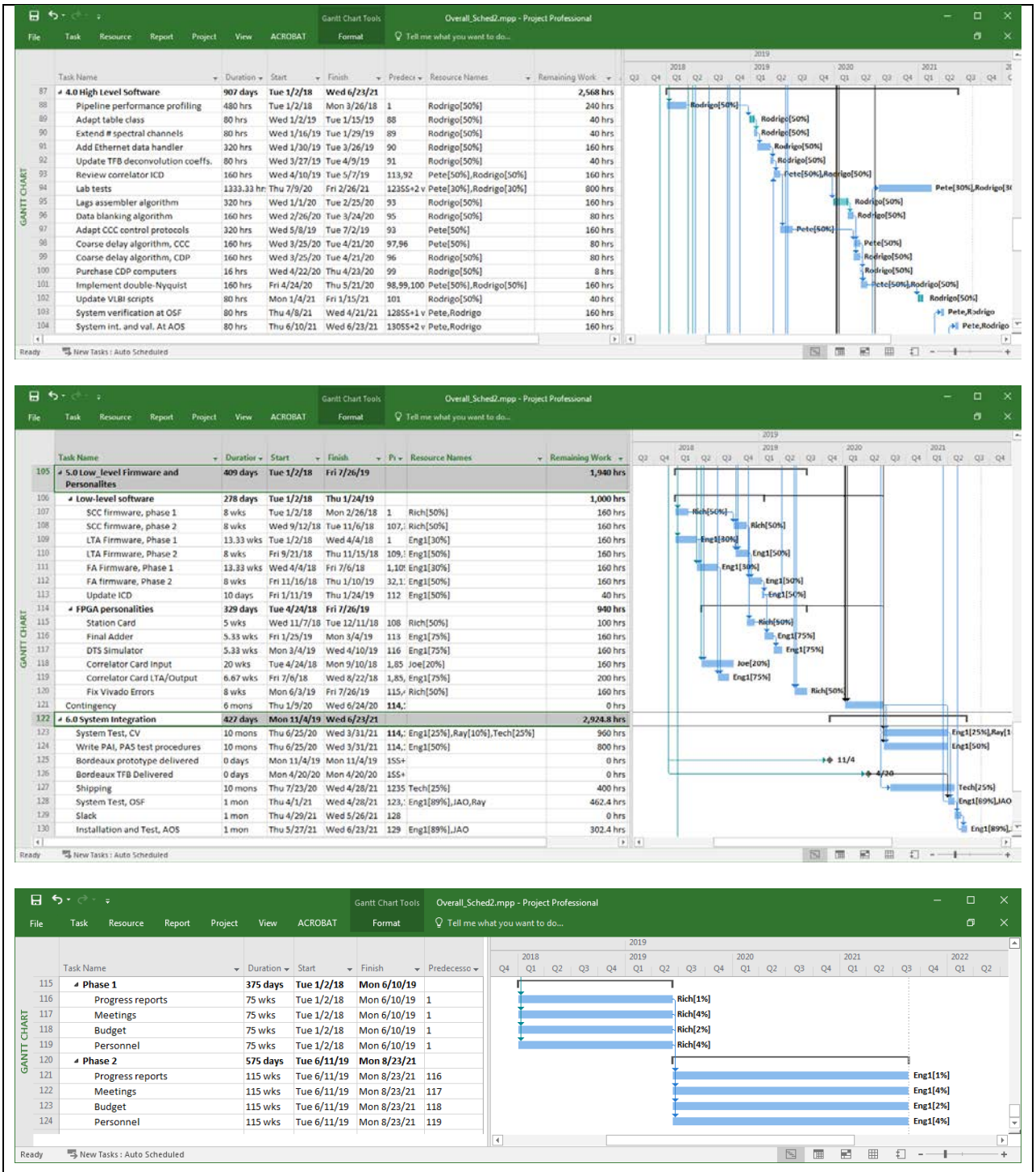

Figure 1.0: Project Schedule.

11.0 Project Management

11.1 Systems/Configuration Control

11.1.1 Systems Requirement and Specification Control

Development engineering and design activities will be conducted in accord with established ALMA Systems Engineering policies, practices and procedures.

11.1.2 Documentation Control

All shared documents will be dated and bear a revision level number.

11.1.3 Product & Quality Assurance Control

Development engineering and design activities will be conducted in accord with established ALMA PA/QA policies, practices and procedures. A unique Product Assurance Plan is unnecessary.

11.2 Performance to Schedule

The Principal Investigator has primary responsibility for schedule development and performance to schedule. The NA ALMA Development Program office will provide support to the PI in establishment of a revision-controlled Project schedule and monthly preparation of performance to schedule status. In the event of a schedule variance, the PI and the NA ALMA Development Program Manager will assess the impact and develop the appropriate recovery action(s).

11.3 Performance to Budget

The Principal Investigator has primary responsibility for intra-project budget allocation and cost performance. The NA ALMA Development Program office will provide support to the PI in establishment of cost accounts, budget load, and the preparation of a revision-controlled, monthly Budget Status Report. In the event of a cost variance, the PI and the NA ALMA Development Program Manager will assess the impact and develop the appropriate recovery action(s).

11.4 Measures of Success

The first-generation correlator went through extensive testing to assure that the delivered product met its specifications. Some of this testing was formally documented and some was not, being done during development as standard good practice. Formally documented hardware tests include "Provisional Acceptance In-house" (PAI) and "Provisional Acceptance at Site" (PAS). These test procedures are available on ALMA EDM:

http://edm.alma.cl/forums/alma/dispatch.cgi/iptdocscorr/showFolder/100603/def/def/4983307

http://edm.alma.cl/forums/alma/dispatch.cgi/iptdocscorr/showFolder/100609/def/def/5896023

They were carried out for each quadrant as it was delivered. A higher level test procedure was executed once all four quadrants were in place:

http://edm.alma.cl/forums/alma/dispatch.cgi/iptdocscorr/docProfile/100788/

Similarly, software testing is tracked using ALMA's JIRA system, in cooperation with the ALMA commissioning scientists. See, for example

http://jira.alma.cl/browse/COMP-5877

A similar approach, PAI plus PAS and JIRA tracking plus commissioning by ALMA is planned for the correlator upgrade. In addition, the test approach includes testing at the OSF using a "Fifth Quadrant". This will allow operation of a representative part of the correlator with live telescopes and may uncover subtle errors before any modifications are made to the existing correlator at the AOS. Testing on the sky was much easier as successive quadrants of the original correlator were delivered since ALMA was then mostly in a development and commissioning mode. Now that ALMA is primarily in science production, we feel that the additional testing at the OSF will maximize the chance of success once the correlator at the AOS is upgraded.

At the hardware level, the correlator is designed with many built-in test features. These permit rapid isolation of faults and an efficient way to test various subsystems. These built-in tests are routinely used in the weekly maintenance of the first-generation correlator. In addition, special cards to simulate telescope data can be inserted into the system in place of the Data Receiver Cards which interface to the optical data transmission system. These were very instrumental in testing the first-generation correlator both in Charlottesville and at site. Our plan includes the design of an upgraded version of this test card to provide powerful, fairly realistic test capabilities before the upgrade leaves Charlottesville.

Specifications for the upgraded correlator are included in Appendix A. Testing will be conducted against these specifications.

On-time and on-budget delivery are also key measures of success. Many of the engineers involved in the design and testing of the current correlator are involved in the upgrade. Thus cost and schedule estimates are based on knowledge gained from a very similar project. The upgrade project will be managed for on-time and on-budget delivery.

11.5 Risk Management

The overall risk of this project is low. This is due to several factors. First, the team is very experienced with correlators in general and with the ALMA correlator in particular. Many of the engineers who designed the current ALMA correlator are included on the upgrade design team. Second, a great deal of the design work has already been done during the course of the ALMA Development Cycle 3 study, "Spectral Line Resolution & Bandwidth Upgrade of the ALMA Correlator". This allowed the team to get very realistic estimates for cost and schedule. Third, the team proposing to do the complementary project of upgrading the samplers, data transmission system and Tunable Filter Banks (TFB) (Laboratoire d'Astrophysique de Bordeaux, Univ. Bordeaux) designed the sampler and TFB designs in the current ALMA system.

Table 9.0: Project Risk Assessment.

NO.	PRIMARY RISK(S)	PROB. (%)	IMPACT ($)	MITIGATION
1	Dependency on Universite de Bordeaux project funding for complementary effort	20%	250K	This project has dependencies on a separate Universite de Bordeaux project that is also seeking funding. If the complementary sampler upgrade cannot be synchronized with the correlator upgrade, it is possible to do the correlator upgrade in two phases. First, the resolution could be increased. This could be followed later by the bandwidth increase. An overall schedule delay of six months has been estimated but would be subject to the timing of complementary project funding.
2	Production ASIC fails due to NRAO technical error	10%	$2M	NRAO will select a competent vendor who is easy to communicate with. Conduct extensive tests in simulation and during two rounds of prototypes.
3	Doubling the clock rate in the infrastructure fails	10%	$50K	Conduct extensive tests prior to the start of the project.
4	Key resource may retire during the life cycle of the project	90%	NA	Bring in apprentices early in the project to ease the transition. Ask the experienced designers to stay on. Transition to a new PI is built into the project schedule. Because the overlap is built into the project, the contingency is set to zero.

5	Engineer allocated to correlator card design and system testing is retired and part time (20%)	20%	50K	It is unlikely that an engineer could be hired to fill a 20% vacancy for a few years. There are two real ways to mitigate this risk: divert other local staff to do the tasks and extend the project by a few months. This risk is balanced by the zero probability that this engineer would take a job elsewhere.
6	A key resource, allocated to over 1300 hours on the project, is not under contract to NRAO and is volunteering his time as an in-kind contribution.	20%	85K	Additional staff would have to be hired to replace this resource. Due to resource's high level of expertise, and the time required to hire a replacement, his departure would extend the project by up to 6 months. This risk is balanced by the zero probability that this engineer will take a job elsewhere, a 31 year excellent track record as an NRAO employee and 10 year record as a volunteer.
7	PCB design errors may require a "re-spin"	10%	20K	Time for some re-spins is built into the schedule.
8	RFI emission from the correlator may exceed ALMA limits.	1%	200K	ALMA decided against shielding the correlator room when building the AOS technical building. This decision was likely based on the fact that the antennas are remote and that the main vulnerability to RFI is via the receivers. An upgraded correlator may be a factor of two worse in RFI spectral content. Measurements of the current correlator showed measurable RFI, from a test antenna located about 5 m from the correlator, up to about 8 GHz, plus a component at 10 GHz due to the DRX cards. The 8 GHz component could potentially double to 16 GHz. The only way to attenuate this would be to shield the room; this would be both difficult and time-consuming.
9	ALMA Downtime during Upgrade	10%	0	Project team is confident the upgrade can take place in a month based on the experience gained in installing the correlator in the first

				place. This type of installation has taken place four times already. The project team will also have practice runs in Charlottesville and at the OSF. However, weather issues are outside of the team's control. If the team is unable to get to the AOS because of weather, then AOS installation and test will take longer. This is an ALMA operational risk.
TOTAL PROJECT CONTINGENCY ($)			**1,219,208**[3]	

11.6 Communication Plan and Progress Reporting

A monthly, "Four-square" progress report will be prepared by the Principal Investigator in accord with Observatory Program Management practices and procedures. Informal reviews will be conducted by the NA ALMA Development Program Manager upon the completion of Level 1 milestones.

12.0 Implementation Plan and Site Location Impact Statement

- Implementation will follow a model similar to the successful model used in the implementation of the 64-Antenna "Baseline" Correlator.
- Hardware will be delivered to Santiago by NRAO.
- Most likely, hardware will be transported to OSF and AOS by JAO at their cost.
- If necessary, NRAO can take care of transportation all the way to the OSF
- JAO personnel will assist with verification testing at OSF (1 FTE month)
- If necessary, an additional month at the OSF can be spent testing the system with the new sampler and DRX designs.
- JAO personnel will assist with testing at AOS (2 FTE month). (This will serve as training to familiarize them with the system upgrade. Currently used diagnostics will look very similar in the upgraded system.)
- Software testing will follow the usual ALMA software testing approach.
- NRAO personnel will assist with commissioning as necessary, but this is primarily a JAO responsibility.

[3] Overall risk value is $2,655,000 with an average probability percentage of 20%. An overall project contingency of 15% has been added to cover potential risks.

It should be pointed out that installation of the upgrade will require a correlator shutdown of approximately one month. Observing time will also be lost to commissioning. However, it should also be pointed out that this lost observing time will be compensated in fairly short order by the efficiency gains provided by the upgrade.

12.1 Implementation Schedule

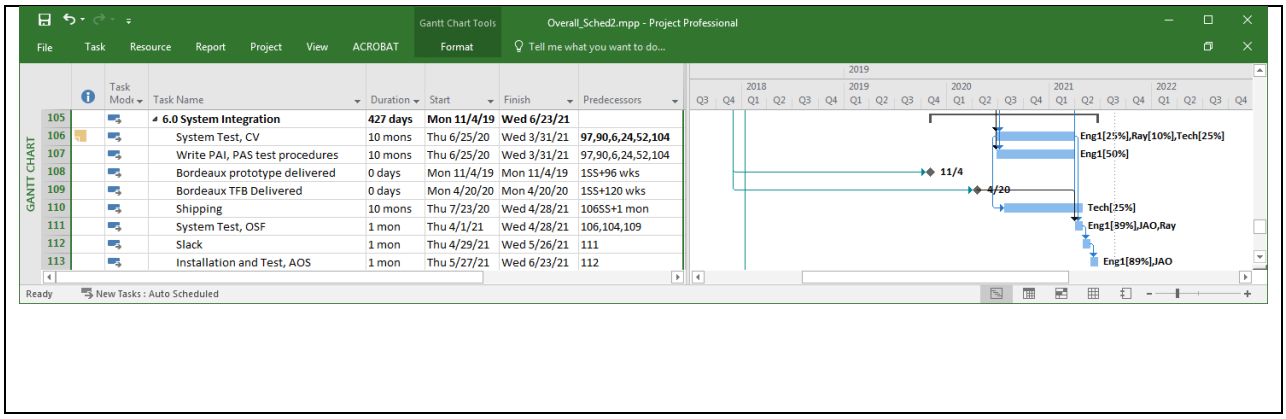

Figure 2.0: Implementation Schedule.

12.2 Site Location Impact Statement

No new facilities or significant modifications to existing facilities are required. Visiting NRAO staff will require lodging, office space and the use of the cafeteria. One-week site visits by NRAO staff in each of the first 3 years of the project are planned for coordination and possibly for non-invasive testing. Two 3 to 4 week visits are planned in the final year of the project.

13.0 Project Closeout

Upon conclusion of this Project, the NA ALMA Development Program Office will coordinate the orderly closeout of activities; or, the transition of activities to implementation. At a minimum, this shall include the following:

- verification of compliance with established procurement policies and procedures;
- verification of Purchase Order final payments;
- verification of compliance with established labor charging practices;
- verification of labor charging accuracy;
- cost and schedule variance analysis;
- resolution of any inventory and/or property control issues;
- inactivation of cost accounts;
- preparation of a Final Report;
- preparation of an Outcome Report; and
- archiving of Project records.

14.0 Commitment

Having read all documents listed in and annexed to the Cycle 5 Call for Project Proposals, and having assessed the situation and the nature and difficulties of the proposed services, the undersigned hereby offers the "***A Significant Upgrade to the ALMA 64-Antenna Correlator***" in accordance with the provisions of the present Call for Project Proposals and, if awarded the Agreement, undertakes to carry out the work required according to best trade practices, within the prescribed time limits, and at the price set out in this Proposal.

Name: __Richard Lacasse_____

Institution: __National Radio Astronomy Observatory_____

Signature:  Digitally signed by Richard Lacasse
Date: 2017.01.30 12:54:06 -05'00'

Date: __January 30, 2017_____

Appendix A – System Specification

The following is excerpted from the system specification generated as part of the PMD-365 Correlator Upgrade Study. "Boiler-plate" information is omitted for clarity and to save space.

Revision History:
2016-Dec-05: Initial Issue
2016-Dec-19: Incorporate Baudry and Escoffier comments
2016-Dec-21: Incorporate additional Baudry comments
2016-Dec-30: Incorporate Amestica and Escoffier comments
2017-Jan-07: Modify VLBI compatibility and High Time Resolution sections; Minor modificatons to LTA Section

ALMA CORRELATOR UPGRADE SPECIFICATION

Introduction and Summary

This document describes the ALMA correlator upgrade. The ALMA correlator is a lag correlator with a digital filter bank in the input section of the system that permits it to operate as a digital hybrid correlator. The system can also be operated in a wideband time division mode.

Overall system specifications for the ALMA correlator can be seen in Table 1.

Table 1. ALMA Correlator Specifications

Item	Specification
Number of antennas	64
Number of baseband channel inputs per antenna	8
Input sample format	3 bit, 8 level at 8 GSample/s per baseband channel
Correlation sample format	2 bit, 4 level and 4 bit, 16 level; Nyquist and twice Nyquist
Maximum baseline delay range	300 km***
Hardware cross-correlators per baseline*	262,144 leads + 262,144 lags
Hardware autocorrelators per antenna*	262,144
Typical performance in digital hybrid modes	32768 spectral points provided for each pair of baseband inputs**
Product pairs possible for polarization	HH, VV, HV, VH (for orthogonal H and V)

* 125 MHz correlators (250 MHz clock rate), divide by 32 to get number of equivalent 4 GHz correlators
** Resulting in 65536, 32768 or 16384 spectral points across the baseband spectrum, depending on polarization mode
***the design of the current correlator can also accommodate 300 km baselines, but this was not included in the original specification. Using longer baselines may require new approaches to updating delays due to the high delay rates for long baselines.

The ALMA correlator evolved from an initial system design (described in ALMA memos 166 and 194) with a pure lag architecture incorporating simple FIR digital filter cards (described in ALMA memos 204 and 248) to a design implementing a digital hybrid correlator with the incorporation of 32-element digital filter bank cards.

The fundamental change to the original design, the replacement of the digital filter card with a tunable filter bank card, is based on the design philosophy of the proposed '2nd Generation Correlator' system (and is described in ALMA memo 476). The use of a 32-element filter bank instead of a single digital filter has the effect of increasing the performance of the system by factors of up to 32 in spectral resolution.

A single wideband time-packet or time-division mode of the original system design has been retained in the operation of the correlator to provide high time resolution where this parameter is of highest importance.

The ALMA correlator upgrade evolved from a need to provide ALMA with additional processing power approximately 15 years after the start of the original design. The upgrade uses the original infrastructure (racks, power, clock distribution, cooling). It replaces cards in the data chain with new cards that run at 250 MHz (internally generated from the provided 125 MHz). Additionally, it replaces the original correlator chip with one that has 32 times the processing power (8 times as many lags per antenna pair and 4 times the number of antenna pairs). The resulting system processes twice the bandwidth of the original 64-Antenna Correlator and produces 8 times as many spectral points.

Applicable and Reference Documents

Applicable Documents List (ADL)

The following documents, with the revision in force as of the date of this specification, form part of this SOW. In the event of conflict between the documents referenced here and this document, this SOW shall take precedence, except for ICDs which clearly need to be re-written.

No.	Document Title	Reference
AD 01	ALMA Product Assurance Requirements	ALMA-80.11.00.00-001-B-GEN
AD 02	ALMA System Electromagnetic Compatibility Requirements	ALMA-80.05.01.00-001-B-SPE
AD 03	ICD between Site and Correlator	ALMA-20.00.00.00-60.00.00.00-A-ICD
AD 04	ICD between Back-End and Correlator	ALMA-50.00.00.00-60.00.00.00-A-ICD
AD 05	ICD between Correlator and Computing Correlator Software	ALMA-60.00.00.00-70.40.00.00-A-ICD

Reference Documents List (RDL)

No.	Document Title	Reference
RD 01	ALMA Project Plan, Version II	Dated September 23rd, 2004
RD 02	ALMA Design Reviews - Definitions, Guidelines And Procedures	ALMA-80.09.00.00-001-B-PLA
RD 03	ALMA Product Tree	ALMA-80.03.00.00-001-M-LIS

Definitions, Abbreviations and Acronyms

AD	Applicable Document(s)
ADL	Applicable Documents List
ALMA	Atacama Large Millimeter Array
AOS	Array Operations Site
CCC	Correlator Control Computer
CDP	Correlator Data Processing computer
Corr	Correlator
DTS	Data Transmission System
ESO	European Southern Observatory
ICD	Interface Control Document
IPT	Integrated Product Team
JAO	Joint ALMA Office
LAB	Laboratoire d'astrophysique de Bordeaux
LTA	Long Term Accumulator
NRAO	National Radio Astronomy Observatory
NTC	NRAO Technology Center
OSF	Operations Support Facility
QCC	Quadrant Control Card
RDL	Reference Document(s) List
SCC	Station Control Card
SOW	Statement of Work
TB	AOS Technical Building
TFB	Tunable Filter Bank

System Block Diagram

A block diagram of the ALMA correlator can be seen in Figure 1. Changes resulting from the upgrade are highlighted in green. This figure also includes some details of the ALMA digitizers, the DTS transmission system, and the real time computer and although these components of ALMA are not part of the correlator they are shown here for clarity.

The input stage of the correlator is the tunable filter bank card. This card is driven by the output of the ALMA DTS receiver/demux card which recovers the 3-bit (or possibly 4-bit, to be determined) samples generated by the ALMA digitizer and sent via optic fiber from the remote antennas over the ALMA Digital Transmission System. The filter bank card can be configured as 32 digital filters with either 125 or 62.5 MHz bandwidth, depending on selected pre-calculated taps in the last stage of the decimation filter. The center frequency of each filter is independently tunable.

The station card has several functions with the main ones being the implementation of bulk delay for geometric delay adjustment and being a router between the filter card outputs and the correlator inputs. Programming in the station cards determines how the 32 filter outputs of the filter card are processed in the correlator system.

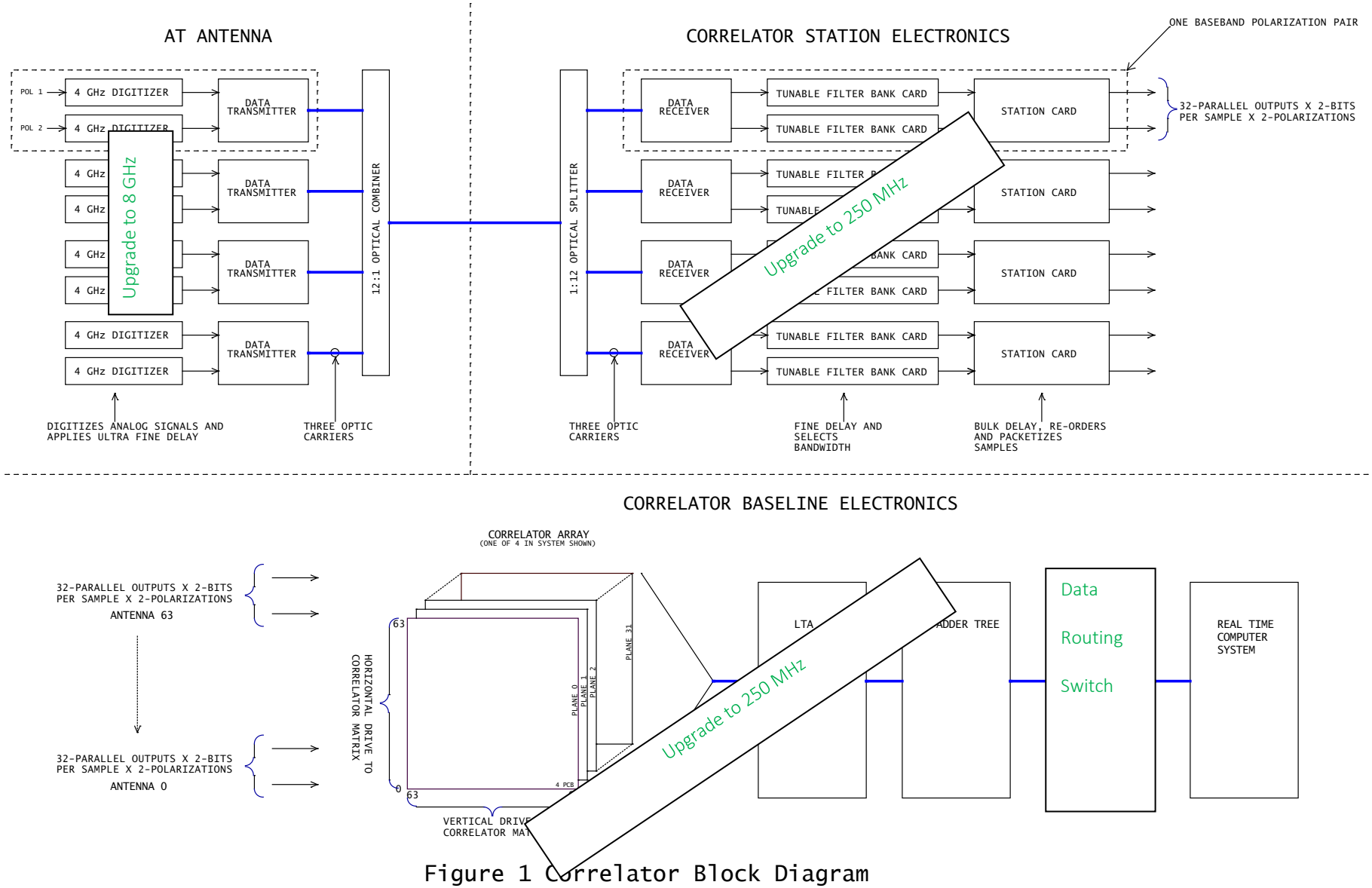

Figure 1 Correlator Block Diagram

The correlator portion of the system consists of 32 correlator planes each implementing a 64-by-64 correlation matrix. When samples from all 64 antennas in the ALMA main array drive this matrix (both axes), autocorrelations are produced on the matrix diagonal and cross correlations and produced elsewhere (with leads on one side of the diagonal and lags on the other).

The LTA (Long Term Accumulator) subsystem seen in figure 1 takes short, 1 msec integrations output by the ALMA custom correlator chips and provides long term integration for them, up to 1.008 seconds. The LTA also provides the interface into the real time computer system via the Adder Tree and Data Routing Switch.

The ALMA correlator is designed in 4 essentially identical quadrants. Each quadrant processes the output of two of the eight baseband channel outputs of the array. For polarization observations, the two baseband channel outputs processed in a quadrant must be of opposite polarization.

Sub-system Description

Tunable filter bank card

Each 4 GHz IF channel input signal to a filter card consists of 32 time demultiplexed 3-bit (or 4-bit) samples, corresponding to a data flow of 8 GS/s. The basic function of the digital filter card is to develop 32 subchannels from this 4 GHz input as follows. First, the input signal is processed by a complex digital mixer driven by a digital LO to translate each subchannel frequency center to zero frequency. Second, each mixer complex output is sent to 2 parallel filters processing the real and imaginary data streams; each of these 2 parallel filters is implemented in a 3-stage decimation filter described in ALMA memo 579. The first stage is a cascaded integrator comb filter, the second stage is a quarter-band low-pass filter (16 tap-weight) and the third stage is a high performance half-band filter (64 tap-weight) which determines the sub-channel band shape. After decimation and complex to real conversion the signal is 2-bit or, according to the observation mode, 4-bit requantized. Each filter then produces streams of 2- or 4-bit samples at 250 MS/s. (For the correlator upgrade, another digital filter structure somewhat different from that described in memo 579 and using the resources of the latest generation FPGAs is currently under study to implement 32 x 125 MHz sub-bands.)

The 32-filter array allows us to select subchannels with a maximum bandwidth of 125 MHz that can be positioned anywhere within the 4 GHz IF channel. One may also select a 62.5 MHz bandwidth with an oversampling option.

It is anticipated that the TFB and the DRX functionality will be integrated into one card which will be installed in the original DRX slot. As the project is presently conceived, this part of the correlator upgrade will be provided by the Laboratoire

d'Astrophysique de Bordeaux group (LAB), Univ. de Bordeaux with ESO support. (The remaining parts of the upgrade as well at the system integration will be the responsibility of the NRAO.) The card will draw power and timing signals from the backplane while interfacing to the Station Card via a rigid-flex cable that bypasses the original backplane connections. Each filter communicates with the station bin control computer via a standard CPLD interface chip; this interface is also carried on the rigid-flex cable. This interface allows the system to monitor the FPGAs and to download the FPGA personalities (bandwidths and filter shapes are selected using precalculated filter tap weights). Unlike in the original system, the FPGA personalities will be stored on the DRX/TFB card instead of the Station Control Card.

In addition to the filter array and to the CPLD interface, fine delay for the input bitstream is implemented on the card. The fine delay increments are operated in synchronism with the bulk delay implemented in the Station Cards.

Station Card

Each Station card provides two 4-millisecond RAM buffers, one for each of two filter card outputs (that is, each buffer holds approximately 4 milliseconds of samples at the full 8 GHz sample rate of a single baseband channel output). A station card provides several basic functions in the correlator:

Provides bulk storage of the geometric delay adjustment
Provides a versatile cross bar function between the filter card output and the correlators
Provides lag generation for high frequency resolution modes
Generates time packets of samples in time division mode

The two basic modes of the station card reflect the two operation modes of the ALMA correlator. Most observations will use the high frequency resolution digital hybrid configuration. In these cases, the input to the station card from a filter card(s) consists of from 1 to 32 separate bands each with a 250 MHz clock rate (either Nyquist sampled or twice Nyquist sampled for the oversampled modes of table 2, 3, and 4).

The other operating mode of the correlator is used in high time resolution observations. In this mode, the filter cards provide a pass through function and the station card input is the full 8 GHz clock rate output of the ALMA digitizer(s) (with samples limited to 2-bits). In this mode, each one millisecond of the full bandwidth signal at the station card input is split into 32 one millisecond packets, each with a 250 MHz clock rate, in the station card RAM buffer. The 32 packets are routed to 32 correlator planes (see below) where cross correlation occurs.

Correlators

The basic building block of the correlator system is a matrix of 64-by-64 correlator blocks referred to as a correlator "plane". A correlator plane provides a 2048 lag correlator circuit at each of the intersections of the matrix (a correlator plane thus has 64x64x2048 total correlator lags). Each 2048 lag circuit is driven by two different polarization signals from each of two antennas and can be programmed to be a single 2048-lag block, to be two 1024-lag blocks, or to be four 512-lag blocks to support the various polarization options. For 2048 lag blocks on the diagonal of the matrix, the two antennas are the same and these yield autocorrelation results.

The next building block of the correlator system is the correlator "array" which consists of 32 correlator planes. There is one correlator array in each correlator quadrant and this array can process the full 4 GHz bandwidth for all 64 antennas for 2 baseband channels.

In the widest bandwidth (digital hybrid) mode, each of the 32 filter card outputs is processed in one of the 32 correlator planes of a correlator array (each filter card output will typically be a 125 MHz sub-band, Nyquist sampled with a clock rate of 250 MHz). For narrower bandwidth modes, some filter card outputs are not processed and the freed-up correlator planes are used to develop additional lags from the active filter card outputs. Lag generation for these modes is done on the station card.

In time division observations, the 32 correlator planes in a quadrant process the 32 time bins developed by the station card. Thus each plane handles 1/32 of the samples taken by an antenna digitizer and the 32 planes correlating station card time packet outputs with a 250 MHz clock rate keeps up with the 8 GHz original sample rate.

LTA subsystem, Final Adder and Data Routing Switch

The Long Term Accumulators provide buffers, or longer term integration, for correlator chip results. The new ALMA2 correlator chips have built-in integrators. This allows the number of lags to be traded for time resolution in the correlator chip. Time resolutions of 16, 8, 4, 2 and 1 msec are possible with this scheme. Data are dumped from the correlator chips to the LTA on 16-msec boundaries. In the upgrade, it is anticipated that the Long Term Integration functionality will be implemented on the same card that contains the correlator chips.

The LTA Adder Tree functionality shown in Fig. 1 is implemented on the Final Adder cards. There are two such cards in each quadrant. The Final Adder cards have several purposes. First, each card adds the results of up to 32 correlator planes for modes where multiple correlator planes must be added together. Second, the Final Adder cards provide the necessary multiplication (shifting) and addition of correlator results in planes that require this operation for support of 16 level correlation. Finally, The Final Adder cards packetize the data into 10 GbE frames for transmission to the CDP cluster via a Data Routing Switch, a commercial Ethernet SFP+ Switch. This allows auto-correlations to be distributed to all CDPs by multicast. The switch also performs the

functions of the original cross-bar in the Final Adder, routing required sets of correlation results to the required CDPs.

The control functionality of the original LTA will remain.

Control cards

There are three types of control cards in the correlator system.

- Station control card (SCC)
- LTA/Correlator control card (LTA/CCC)
- Quadrant control card (QCC)

Each correlator system control card has a 16-bit Infineon C167 microprocessor that communicates with the correlator control computer over a serial CAN bus. The SCC and LTA/CCC control cards each support an 8-bit bidirectional communication bus over the bin motherboard to individual logic cards in the system. This bus is used for control and monitoring functions such as FPGA personality loading, mode programming, active observation support, and various monitoring responsibilities. The QCC monitors voltages and temperatures in the system and can force a power down when a danger is detected.

Software for the ALMA correlator control cards is written in C using a Keil software development system.

The correlator upgrade will retain the same control system. This leverages the many FTE-years of work that went into developing software and control protocols. It is expected that only minor control software changes will be required for the upgrade.

Performance

The performance of the ALMA correlator, in terms of bandwidth and frequency resolution, can be seen in the next three tables. Table 2 gives the performance of a single quadrant of the correlator in modes in which a single baseband channel of a baseband pair is processed. In the original correlator, it was found that this mode was not useful because astronomers *always* want to look at both polarizations. Thus, if ALMA agrees, the modes in Table 2 will be implemented for posterity but will not be formally tested as part of the acceptance procedure. Table 3 gives system performance in modes in which both baseband channels of a pair are processed but no cross correlations are performed. Table 4 gives the system performance in modes in which polarization cross correlations are generated.

The sensitivity column in tables 2, 3 and 4 does not reflect the initial ALMA 3-bit digitizer contribution to sensitivity but only the correlator efficiency after the 2-bit or 4-bit requantization at the filter output. Also, optimum sampler levels are assumed.

The spectral resolution of frequency division modes (FDM) scales by a factor of 8 for all modes from the original design to the upgrade design due to the additional lags present in the new correlator chip, the ALMA2. However, the spectral resolution of time division modes (TDM) does not scale this way. The spectral resolution of TDM modes is limited to 512 lags by the need to limit the loss due to "blanking time". Higher TDM resolution would cause undesirable efficiency loss in both FDM and TDM.

Size and Power Requirements

Each quadrant of the correlator consists of eight digital racks, one power supply rack and one computer rack. Four of the digital racks house DRX/TFB cards, and station cards sufficient to process the output of two of the 8 baseband channels produced by 64 antennas of the ALMA array. The other 4 racks house a single correlator array and LTA/CCC cards.

Power requirements are expected to be about 40 kW per quadrant including the DRX/TFB cards. Power dissipation of the upgraded correlator is expected to be less than that of the original correlator.

Phasing System Compatibility

Compatibility with the existing VLBI system will be maintained. In discussions with the VLBI community have established that a different mode can be used so long as it results in the same bandwidth and data rate. The mode must be a cross-polarization mode. Mode 14 in table 4 is the mode that has been selected for compatibility. This mode will require that the Phasing Interface Cards (PICs) be updated so that their personality runs at 250 MHz.

High Time Resolution Modes

The recent peak of interest in Fast Radio Bursts (FRBs) has prompted a request that the correlator upgrade consider adding features that would enable high time resolution observations. This feature would also be useful in other transient detection fields of astronomy such as solar and pulsar. Since this is a recent request, requirements, much less a design, for this feature have not solidified. There are a range of possible designs, each with advantages and disadvantages. Our plan is to continue discussion with the astronomy community while evaluating requirements and design options. At a minimum, 1-msec time resolution with 32 antennas, single polarization and 128 spectral points will be designed into the hardware. An option to add a 10 GbE connection to every correlator card has been costed into the correlator card as a "place holder". This would allow for a later upgrade that would connect the correlator cards to a cluster of computers. The needs of the scientific community will be studied during 2017 and a final design decided before the start of the project.

Table 2 Mode chart with one baseband channel per quadrant being processed (PAS testing to be confirmed)

Mode #	Number of sub-channel filters	Total Bandwidth	Number of Spectral Points	Spectral Resolution	Velocity resolution at 230 GHz	Correlation	Sample Factor	Minimum dump time[1]	Sensitivity[2]
1	32	4 GHz	65536	61 kHz	0.08 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
19	32	4 GHz	32768	122 kHz	0.16 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
38	32	4 GHz	16384	244 kHz	0.64 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
2	16	2 GHz	65536	30.5 kHz	0.04 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
20	16	2 GHz	32768	61 kHz	0.08 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
39	16	2 GHz	16384	122 kHz	0.16 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
53	16	2 GHz	8192	244 kHz	0.64 km/s	4-bit x 4-bit	Twice Nyquist	64msec	0.99
3	8	1 GHz	65536	15.3 kHz	0.02 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
21	8	1 GHz	32768	30.5 kHz	0.04 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
40	8	1 GHz	16384	61 kHz	0.08 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
54	8	1 GHz	8192	122 kHz	0.16 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
4	4	500 MHz	65536	7.5 kHz	0.01 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
22	4	500 MHz	32768	15.3 kHz	0.02 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
41	4	500 MHz	16384	30.5 kHz	0.04 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
55	4	500 MHz	8192	61 kHz	0.08 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
5	2	250 MHz	65536	3.75 kHz	0.005 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
23	2	250 MHz	32768	7.5 kHz	0.01 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
42	2	250 MHz	16384	15.3 kHz	0.02 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
56	2	250 MHz	8192	30.5 kHz	0.04 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
6	1	125 MHz	65536	1.9 kHz	0.0025 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
24	1	125 MHz	32768	3.75 kHz	0.005 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
43	1	125 MHz	16384	7.5 kHz	0.01 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
57	1	125 MHz	8192	15.3 kHz	0.02 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
25	1	62.5 MHz	65536	0.95 kHz	0.00125 km/s	2-bit x 2-bit	Twice Nyquist	512 msec	0.94
58	1	62.5 MHz	16384	3.75 kHz	0.005 km/s	4-bit x 4-bit	Twice Nyquist	128 msec	0.99
68	Time Division Mode	4 GHz	512	7.8125 MHz	10.2 km/s	3-bit x 3-bit	Nyquist	16 msec	1.00
71	Time Division Mode	4 GHz	512[3]	7.8125 MHz	10.2 km/s	2-bit x 2-bit	Nyquist	16 msec	0.88

[1] Assuming all products, all lags, transferred from correlator to Correlator Data Processor computer (in milli-seconds).

[2] Multiply numbers in this column by the 0.96 sensitivity imposed by the 3-bit input digitizer.

[3] 2048 points could be provided, but with an additional noise penalty

Table 3 Mode chart with two baseband channels per quadrant processed with no polarization cross products.

Mode #	Number of sub-channel filters	Total Bandwidth	Number of Spectral Points	Spectral Resolution	Velocity resolution at 230 GHz	Correlation	Sample Factor	Minimum dump time[1]	Sensitivity[2]
7	32	4 GHz	32768	122 kHz	0.16 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
8	16	2 GHz	32768	61 kHz	0.08 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
26	16	2 GHz	16384	122 kHz	0.16 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
44	16	2 GHz	8192	244 kHz	0.32 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
9	8	1 GHz	32768	30.5 kHz	0.04 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
27	8	1 GHz	16384	61 kHz	0.08 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
45	8	1 GHz	8192	122 kHz	0.16 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
59	8	1 GHz	4096	244 kHz	0.32 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
10	4	500 MHz	32768	15.3 kHz	0.02 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
28	4	500 MHz	16384	30.5 kHz	0.04 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
46	4	500 MHz	8192	61 kHz	0.08 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
60	4	500 MHz	4096	122 kHz	0.16 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
11	2	250 MHz	32768	7.6 kHz	0.01 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
29	2	250 MHz	16384	15.3 kHz	0.02 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
47	2	250 MHz	8192	30.5 kHz	0.04 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
61	2	250 MHz	4096	61 kHz	0.08 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
12	1	125 MHz	32768	3.8 kHz	0.005 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
30	1	125 MHz	16384	7.6 kHz	0.01 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
48	1	125 MHz	8192	15.3 kHz	0.02 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
62	1	125 MHz	4096	30.5 kHz	0.04 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
31	1	62.5 MHz	32768	1.9 kHz	0.0025 km/s	2-bit x 2-bit	Twice Nyquist	512 msec	0.94
63	1	62.5 MHz	8192	7.6 kHz	0.01 km/s	4-bit x 4-bit	Twice Nyquist	128 msec	0.99
69	Time Division Mode	4 GHz	512[3]	7.8 MHz	10.2 km/s	2-bit x 2-bit	Nyquist	16 msec	0.88

[1] Assuming all products, all lags, transferred from correlator to Correlator Data Processor computer (in milli-seconds).

[2] Multiply numbers in this column by the 0.96 sensitivity imposed by the 3-bit input digitizer.

[3] 1024 points could be provided, but with an additional noise penalty and a time resolution penalty

Table 4 Mode chart with two baseband channels per quadrant processed with polarization cross products.

Mode #	Number of sub-channel filters	Total Bandwidth	Number of Spectral Points	Spectral Resolution	Velocity resolution at 230 GHz	Correlation	Sample Factor	Minimum dump time[1]	Sensitivity[2]
13	32	4 GHz	16384	244 kHz	0.32 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
14[3]	16	2 GHz	16384	122 kHz	0.16 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
32	16	2 GHz	8192	244 kHz	0.32 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
15	8	1 GHz	16384	61 kHz	0.08 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
33	8	1 GHz	8192	122 kHz	0.16 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
16	4	500 MHz	16384	30.5 kHz	0.04 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
34	4	500 MHz	8192	61 kHz	0.08 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
17	2	250 MHz	16384	15.3 kHz	0.02 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
35	2	250 MHz	8192	30.5 kHz	0.04 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
51	2	250 MHz	4096	61 kHz	0.08 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
18	1	125 MHz	16384	7.6 kHz	0.01 km/s	2-bit x 2-bit	Nyquist	512 msec	0.88
36	1	125 MHz	8192	15.3 kHz	0.02 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.94
52	1	125 MHz	4096	30.5 kHz	0.04 km/s	4-bit x 4-bit	Nyquist	128 msec	0.99
66	1	125 MHz	2048	61 kHz	0.08 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.99
37	1	62.5 MHz	16385	3.8 kHz	0.005 km/s	2-bit x 2-bit	Twice Nyquist	512 msec	0.94
67	1	62.5 MHz	4096	15.3 kHz	0.02 km/s	4-bit x 4-bit	Twice Nyquist	128 msec	0.99
70	Time Division Mode	4 GHz	512	7.8 MHz	10.2 km/s	2-bit x 2-bit	Nyquist	32 msec	0.88

[1] Assuming all products, all lags, transferred from correlator to Correlator Data Processor computer (in milli-seconds).

[2] Multiply numbers in this column by the 0.96 sensitivity imposed by the 3-bit input digitizer.

[3] VLBI compatibility mode using 16 x 125 MHz filters

Appendix B – System Modification Overview

This appendix describes the upgrade to the 64-antenna ALMA correlator from the system level. It was written as part of the ALMA Correlator Upgrade Study. An overview of the changes to the original system is presented as well as reviews of all the design work performed so far.

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Introduction

The objective of the "ALMA2" upgrade to the 64-antenna ALMA correlator is to double the processed bandwidth of the ALMA system and to increase the spectral resolution of the correlator by a factor of eight. A byproduct of this upgrade will be to increase the observational efficiency significantly in some cases.

The upgrade philosophy is to implement the changes with minimal cost, minimal risk, and minimal disruption to the ALMA system with as much of the current ALMA correlator infrastructure/software/firmware retained as possible.

Doubling the bandwidth and increasing the resolution of the correlator requires the development of a new custom correlator IC roughly 32 times the size of the current ALMA1 ASIC. Fortunately, the increase in the capacity of integrated circuit technology since the design of the original correlator makes this increase possible.

Acronyms

A list of the acronyms used in this document is given below.

ALMA	Atacama Large Millimeter Array
ASIC	Application-Specific Integrated Circuit
BOM	Bill of Materials
CDP	Correlator Data Processor
DPI	Data Port Interface
DRX	Data Receiver (part of DTS below)
DTS	Data Transmission System
FA	Final Adder
FPGA	Field-programmable Gate Array
HVAC	Heating Ventilation and Air Conditioning
LTA	Long Term Accumulator
NRAO	National Radio Astronomy Observatory
QCC	Quadrant Control Card
TFB	Tunable Filter Board
VLBI	Very Long Baseline Interferometry

Study Project Scope

The objective of the ALMA correlator upgrade study (PMD-365) is to produce cost and labor estimates for a modification that will substantially increase the performance of the 64-antenna ALMA correlator. Improvements in the correlator performance include doubling the processed bandwidth and increasing the spectral resolution by a factor of 8. In order to accomplish this objective, a substantial amount of the actual design work required by the upgrade has already been done.

Upgrades to other systems of the ALMA observatory, needed to take full advantage of this correlator expansion, will be listed but not described in detail. One upgrade is particularly noteworthy: the sampling rate at the antennas must be doubled to increase the bandwidth by a factor of two. Since the ALMA system digitizers have to be re-designed, it might be possible to design and install a full 4-bit digitizer-DTS system, yielding an increase in observing sensitivity. For example, an observer currently using mode 1 of the correlator (2 GHz BW, 8192 spectral points across the spectrum, 2-bit X 2-bit sampling) could use upgraded mode 39 (2 GHz BW, 16,384 spectral points, 4-bit X 4-bit sampling) and go from 96% x 88% = 84% sampling efficiency to 99% x 99% = 98% and still get better spectral resolution. A second noteworthy, required upgrade is the Tunable Filter Bank (TFB). This is a correlator module that was designed by Baudry's group at Bordeaux for the current correlator. It is hoped that the same group will design an upgraded TFB to complement the NRAO upgrades to the correlator.

This proposed correlator system enhancement would serve to provide ALMA with an easy, fast, and inexpensive path to enhanced performance, with the expectation of the possible availability of a more versatile software correlator in 10 to 15 years.

The upgrade system will continue to support the phased ALMA interface for VLBI.

"Hooks" will be put into place in the upgrade design for interface to a future transient machine. This interface will allow streaming of raw lag integrations to the external transient system to provide time resolution of 1 msec in FDM and 1/32 msec in TDM.

Project Strategy

The project strategy will be to develop a minimum cost approach in hardware and labor for implementation of the upgrade. Existing hardware and infrastructure, where possible, will be retained unmodified. This includes:

- Racks
- Bins
- Motherboards
- Control cards (the LTA stays as a control card for the correlator bin)
- Power cards (except the correlator mezzanine card)
- Rack-to-rack signal cables
- 48 VDC power supplies

- 125 MHz clock distribution
- Timing Event distribution system

Major items to be re-designed include:

- New ALMA2 custom chip (but not discussed here)
- Replace two TFB cards and one DRX with a new design DRX/TFB card (also not discussed here)
- Replace the station cards with a new design
- Replace SI and CI cards with basically the same design, but using a new FPGA family
- Replace four correlator cards with one new correlator/LTA card using the ALMA2 ASIC
- New correlator mezzanine card
- Replace the final adder card with a new design
- New CDP computer cluster

Correlator control software should be minimally affected since the overall structure of the system will remain unchanged. This is an important cost and schedule savings, given the many person-years of effort that has gone into writing and verifying the correlator control software. Also, because of the higher dump rates contemplated by the upgrade, it may be possible to eliminate the Time Division Modes, resulting in some simplification of the hardware, software, and firmware. Of course, much new firmware will still be required.

As stated above, the correlator clock distribution will be unchanged. The system clock will still be distributed at 125 MHz but will be doubled in the system FPGAs to support the new 250 MHz data rate.

Similarly, DC power distribution will also be unchanged in the system. The low core voltage (0.75 or 1.0 VDC) required by the 28 nm FPGAs to be used in new designs and by the ALMA2 custom chip will require DC-to-DC converters on each new logic card.

The upgrade could be done in two stages (if this were considered useful); first the resolution increase could be made, followed later by the bandwidth increase. This strategy would allow most of the correlator modifications to be made and verified using existing ALMA infrastructure (existing digitizers, DTS, etc.). Later, as upgrades to the ALMA system have been fully verified and became operational, the bandwidth upgrade could be brought on-line.

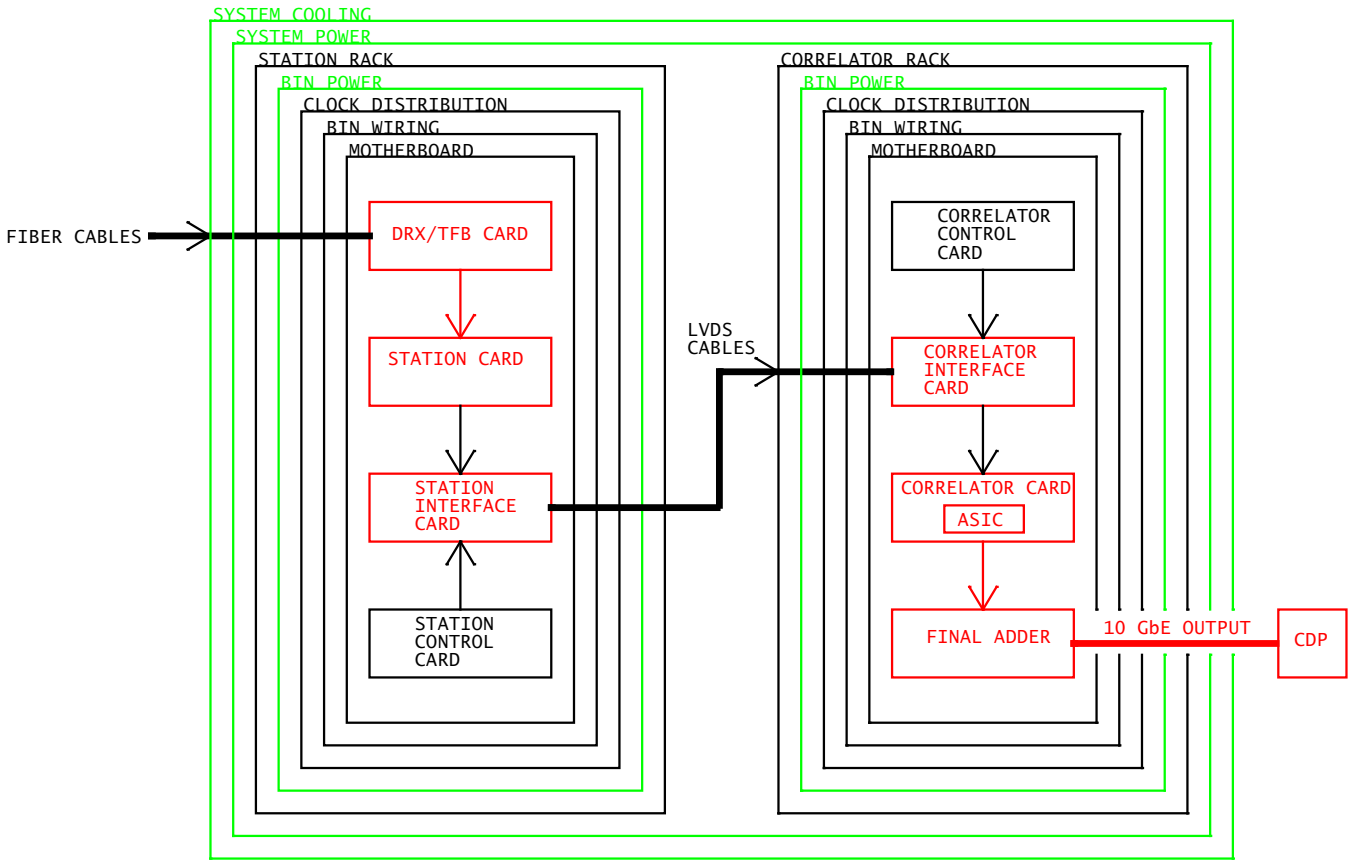
Other changes to the ALMA system will need be made to achieve the full upgrade. Major non-correlator items to be considered include:

- New 4-GHz digitizer and associated changes to the IF system
- New digital transmission system (new DTX and DRX, but no change to the fiber cables or connectors)
- Some IF processor rework including new filters and equalizers to achieve 4 GHz per IF channel digitized

- Revised software to accommodate the increase in bandwidth (for example, delay model tracking, user interface, archive)

Block Diagram

A system block diagram that illustrates the changes needed for the upgrade is seen below. In this figure, features in black remain unchanged in the upgrade while features in red are new designs. Green reflects reductions in requirements.



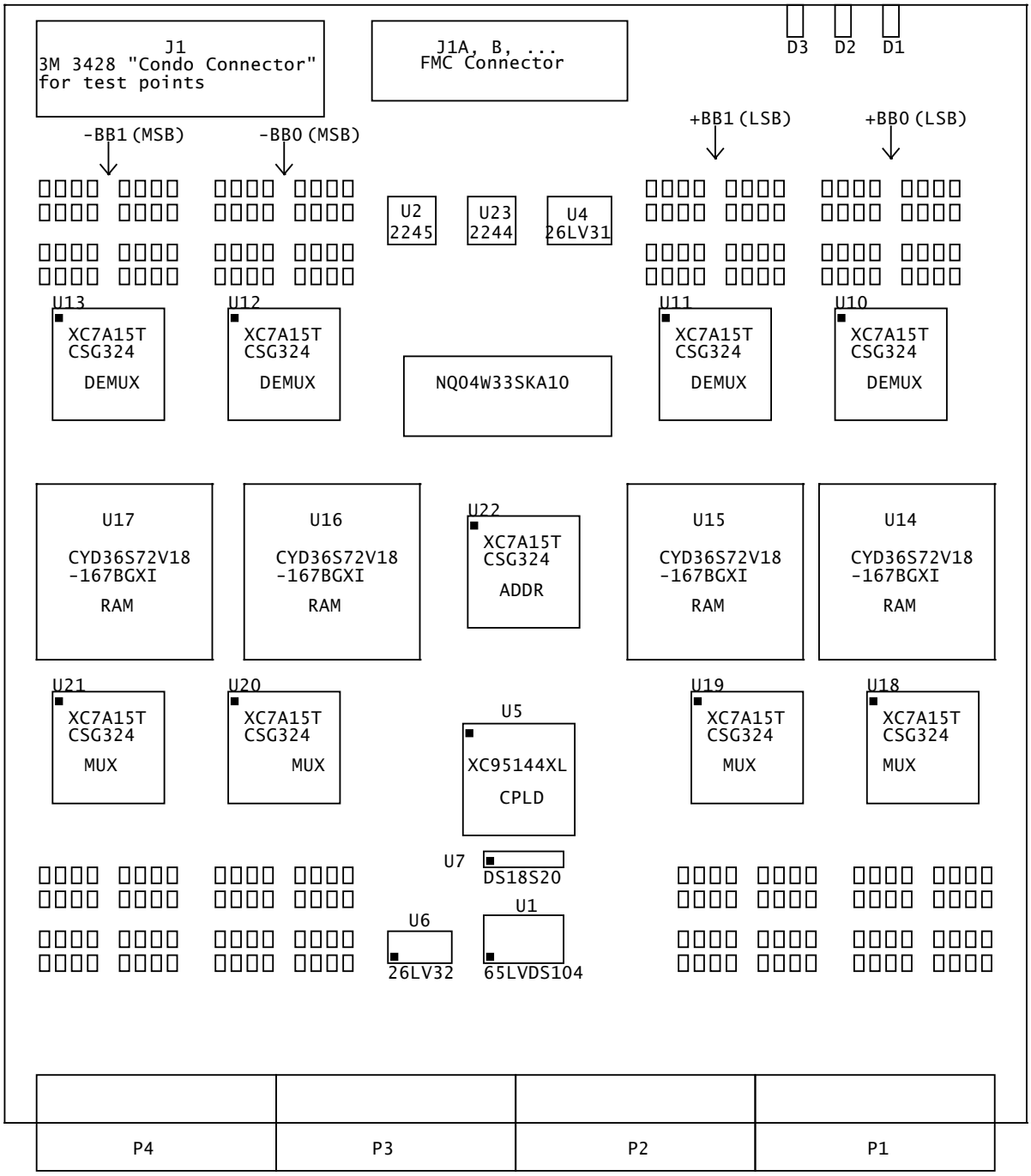
Hardware Considerations

Station Rack Modification Overview

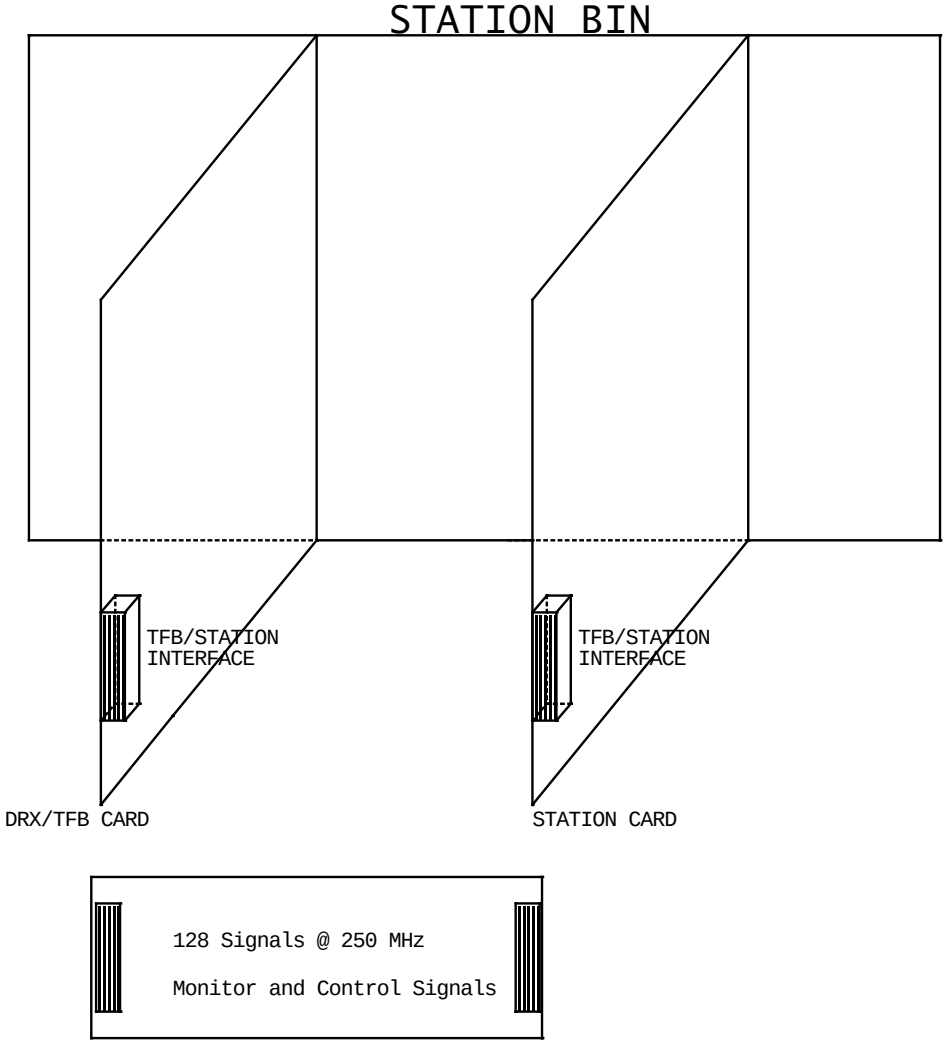
In the station rack, only the SCC, the station power card, and the station motherboard will be retained. A new DRX/TFB card will be required to replace the current DRX and two existing TFB, cards but is not within the scope of this study. It is envisioned that the same group which designed the current generation of TFBs will design the ones for this upgrade using European funds. A new station card will replace the existing station card. A detailed design for the new station card has been made (see [RD1]). A layout sketch of the new station card can be seen below. Note that the signal interface between the DRX/TFB card and the station card is via a card-to-card cable at the top of each PCB. This approach allows the retention of the existing motherboard, saving significant development, testing and installation time.

STATION CARD

6U X 28O EURO-CARD
9.19 " WIDE 11.02" HIGH



As mentioned above, the signal interface between the DRX/TFB card and the station card in the upgrade will be via a card-to-card cable at the top of each PCB. This concept can be seen in the sketch below.



A new DTS simulator card will be developed and use the station card top connector to input test signals into the card or system. The DTS Simulator Card is a very useful test fixture that was used in testing many parts of the ALMA correlator by generating realistic simulated antenna signals with controllable spectral features and controllable correlation coefficients between antenna pairs. Modern FPGAs are such that the entire capability of the old DTS Simulator card can now be fit into a single inexpensive FPGA.

Otherwise, the new station card is a straightforward design. The geometric delay compensation and mode generation functions of the station card shown in the sketch above could use SDRAM instead of static RAM to reduce cost. Elimination of TDM operation, if adopted, will make the design easier.

As stated earlier, the upgrade could be done in two stages. One way to do this is to leave the station racks unchanged and install the resolution upgrade in the correlator racks. An alternate 2-phase strategy would be to install very simple interface cards into the existing TFB cards slots to allow completion of the interface between the existing DRX cards and the new, more complex Station Cards which would also include the TFB functionality. This approach would allow a more complete verification of the full correlator modification before the complete ALMA system is upgraded. The impact to the software and the complexities of the implementation of the 2-stage upgrade should be carefully weighed in the cost/benefit analysis of a 2-stage approach.
Interface Cards and Rack-to-rack Cables
The station rack to correlator rack signal interface remains nearly the same; the LVDS cables currently in place will remain. New SI and CI cards will have to be developed to handle the increased data rate, but except for a new FPGA family, the card and FPGA designs can remain the same (with the exception of including the present SI and CI card discrete LVDS I/O driver/receiver ICs in the new SI and CI FPGAs).

Frequency compensation in the cable interface (by using discrete ICs on the CI card) will be used to improve signal transmission quality in the existing rack-to-rack cables. It is planned that the inclusion of cable equalization will reduce the error rate of the cable system despite the doubling of the data rate.

For operational details of the new SI and CI card designs see in [RD2]. Schematic for the new cards can be seen in [RD3] and [RD4].

Correlator Rack Modification Overview

In the correlator rack, a new correlator/LTA card will replace 4 old correlator cards of a correlator “plane” and provide the first stage of the LTA function.

The 64-chip ALMA2 array on the new correlator card will automatically dump 8,388,608 integration results, 20 bits wide, into the card LTA logic every 16 msec. The content of this dump will be mode dependent (with 1-msec to 16-msec integration times) but the action required by the LTA will not; the LTA logic will integrate lags dumped from the correlators into running sums. The LTA will maintain the 4-bin structure of the current system along with two (integrate/dump) banks.

The maximum dump data rate for long term integrated results from the LTA to the FA will be limited to 1/8 that of the data rate between the correlators and the LTA. This number is a bit arbitrary, but still provides for an output rate from the correlator much higher than at present. The typical output rate from the FA will generally be much lower.

The present LTA card, which also provides the control function for the correlator bin, will control the dump of results from the (new) LTA to the (new) FA as required by the observing mode. If, for example, the observing mode of a given sub-array requires a 256-msec integration period, the bin control card (the old LTA) will supervise the dump of all baselines belonging to this sub-array into the FA every 256 msec as integrations are complete.

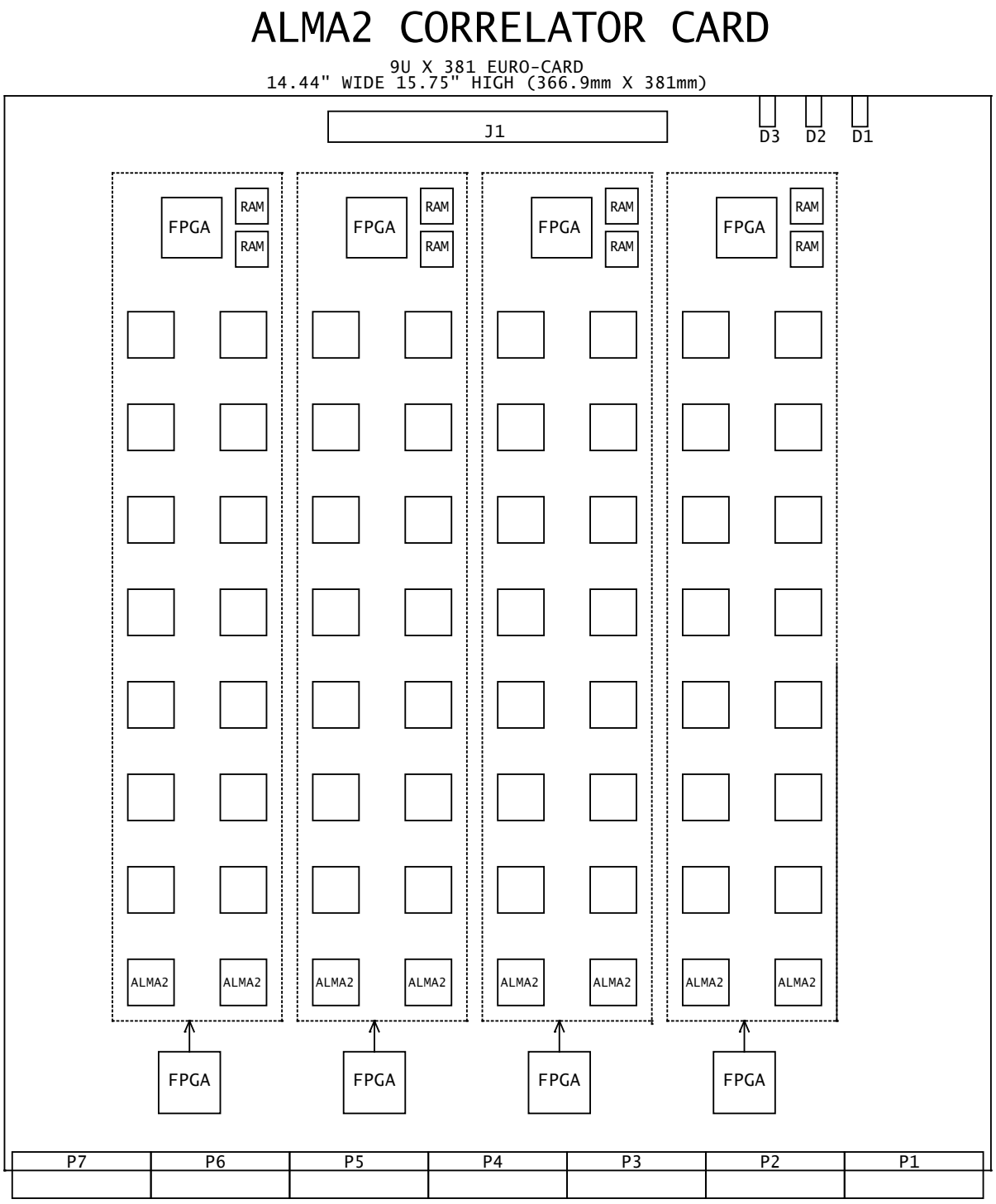
A single FA card will handle the integration results of one correlator rack's 8 correlator cards via card-to-card LVDS cables. The new FA card will go into an existing FA card slot in the system and can use the dedicated 16-bit LVDS inputs of the old FA card. A significant number of new cables will need to be added to enable this. An alternative is to re-use existing cables. However, since these were installed first and are "buried" by the Station Interface to Correlator Interface cables, which were installed later, the current thinking is that the old cables should be unplugged and tied off and new cables installed.

While the LTA native cycle time will remain at 16 msec, sub-cycles in the ALMA2 ASIC will exist at as low as 1 msec. This change eliminates the need for the complicated hardware and firmware support now used for the special 1-msec auto-products only mode. Now 1-msec observations can fit into the normal operation of the system and, in addition, provide cross as well as auto products.

The FA will have to do the final summations to support TDM operation and provide the output of final results into the CDP (Of course, if the system need not support TDM, this card becomes much simpler). Output into the CDP should require four 10-GbE output lines per quadrant.

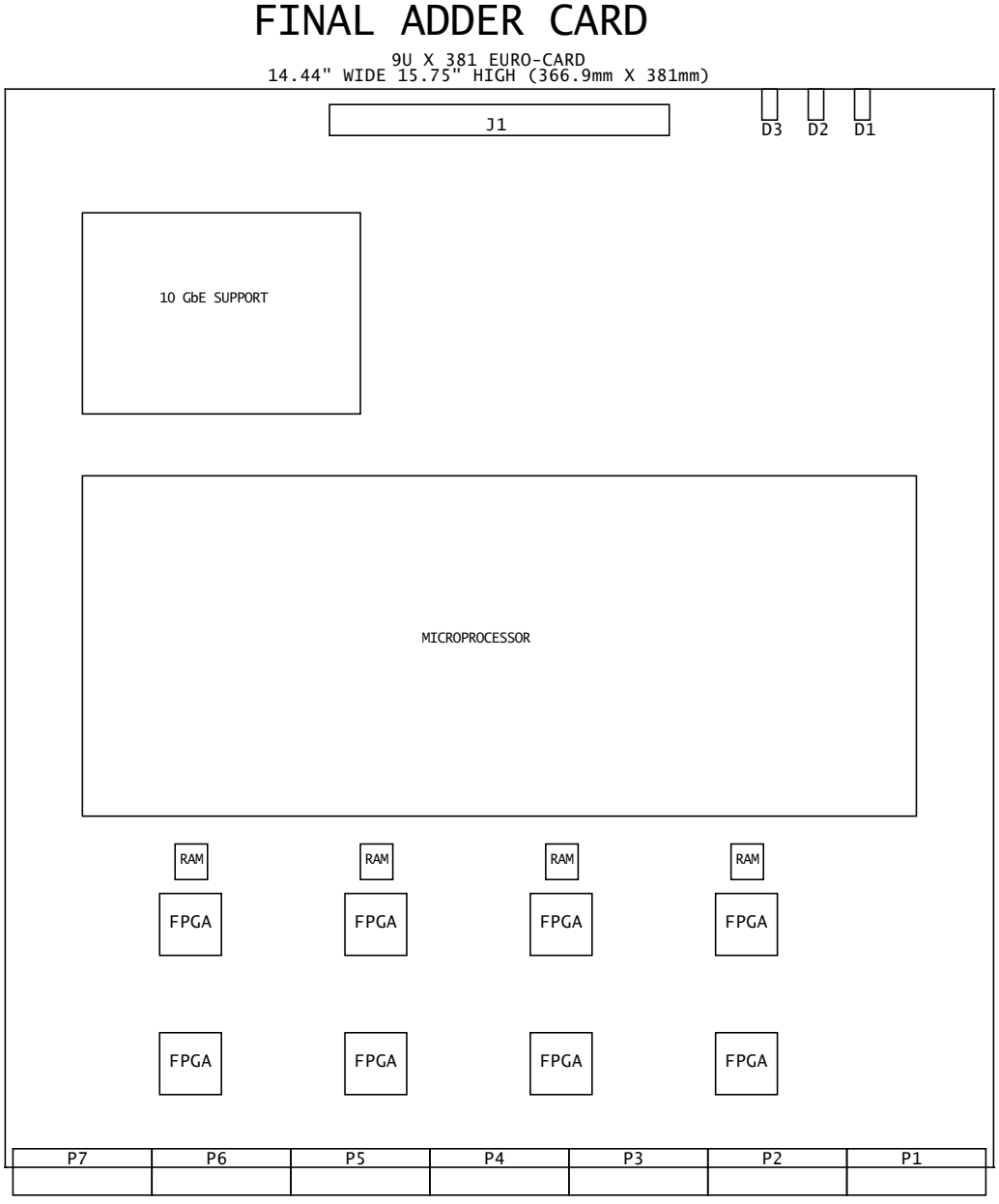
A new correlator power mezzanine card will be needed to supply the lower core voltage of the new ALMA2 ASIC.

A detailed design for the new correlator card has been made; see [RD5] for details. A card layout sketch of the new correlator card is seen below.



The current DPI cards (housed within the computing rack) will not be needed any more since the data transfer from the Final Adder to the CDP cluster will be done by means of 10GbE connection.

A conceptual layout for the new FA card is seen below (note that this card requires a standard ALMA correlator control card function as provided by a system standard C167 microprocessor).



Correlator card schematic

References

[RD01] PMD-365-004-A-SCH Station Card schematic

[RD02] PMD-365-011-A-MAN The SI and CI Card Designs

[RD03] PMD-365-007-A-SCH SI card schematic

[RD04] PMD-365-009-A-SCH CI card schematic

[RD05] PMD-365-017-A-SCH

Appendix C – Summary of Documents Produced for the ALMA Correlator Upgrade Study

The ALMA Correlator Upgrade Study Project was funded in February 2016. The goal of this project was to determine cost and schedule estimates for the proposed correlator upgrade. In order to get accurate cost estimates, the detailed designs of many parts of the system were completed. A large amount of documentation was produced. This documentation, which is expected to be complete by the close of the study in February 2017, is listed in the following table. Reviewers may or may not have access to this documentation. Copies of any of the documents may be requested from the PI.

Document Number	Document Title	Description
PMD-365-001-A-REP	PMD-365 ALMA Correlator Study Project Final Report	Executive summary of detailed reports that follow
PMD-365-002-A-REP	Document Number Assignments	This document
PMD-365-003-A-SCH	ALMA Correlator Upgrade System Overview	Summary of upgrade – what gets changed and how; what does not get changed.
PMD-365-004-A-SCH	Station Card Schematic	Schematic of the Station Card
PMD-365-005-A-BOM	Station Card Bill of Materials	Bill of Material for the Station Card
PMD-365-006-A-MAN	The Station Card Design for the ALMA2 Upgrade	Manual for the Station Card, describing differences from the original design
PMD-365-007-A-SCH	Station Interface Card Schematic	Schematic for the Station Interface Card
PMD-365-008-A-BOM	Station Interface Card Bill of Materials	Bill of Materials for the Station Interface Card
PMD-365-009-A-SCH	Correlator Interface Card Schematic	Schematic for the Correlator Interface Card
PMD-365-010-A-BOM	Correlator Interface Card BOM	Bill of Materials for the Correlator Interface Card
PMD-365-011-A-MAN	The SI and CI Card Designs for the ALMA2 Upgrade	Manual for Station Interface and Correlator Interface cards.
PMD-365-012-A-SCH	ALMA2 ASIC Detailed Block Diagram	Schematic for the ALMA2 ASIC
PMD-365-013-A-DSN	ALMA2 ASIC VHDL Design Files	VHDL code for the ALMA2 ASIC
PMD-365-014-A-REP	ALMA2 ASIC Simulation Report	Simulation report on the ALMA2 ASIC

Document Number	Document Title	Description
PMD-365-015-A-REP	ALMA2 ASIC Proposal Evaluation Report	The study proposal group's evaluation of proposals received for the ALMA2 ASIC
PMD-365-017-A-SCH	Correlator/LTA Card Schematic	Schematic for the Correlator/LTA Card
PMD-365-018-A-BOM	Correlator/LTA Card BOM	Bill of Materials for the Correlator/LTA Card
PMD-365-019-A-SCH	Mezzanine Card Schematic	Schematic for the Correlator Mezzanine Card
PMD-365-020-A-BOM	Mezzanine Card BOM	Bill of Materials for the Correlator Mezzanine Card
PMD-365-021-A-MAN	Correlator/LTA Card Manual	Manual for the Correlator/LTA Card and Mezzanine Card
PMD-365-022-A-SCH	Final Adder Schematic	To be completed in 2017 Produce block diag. for report
PMD-365-023-A-BOM	Final Adder BOM	To be completed in 2017
PMD-365-024-A-REP	Final Adder Manual	To be completed in 2017
PMD-365-025-A-REP	Correlator Data Processor Design and Test Report	Reports on tests of an 8-times increase of data rate into Correlator Data Processor computers
PMD-365-026-A-REP	Plan for Testing New Logic Cards Used in the ALMA Correlator Upgrade	Details the test plan approach at the card level
PMD-365-027-A-REP	250 MHz Correlator Interface Qualification	Reports on tests aimed at checking the viability of doubling the data rate in the existing infrastructure
PMD-365-028-A-REP	Data Rate Testing of the ALMA Correlator	Provides additional detail to PMD-365-020-A-REP.
PMD-365-029-A-REP	Test Results From the test-SI Test PCB	Provides additional detail to PMD-365-020-A-REP
PMD-365-030-A-PLA	Product Assurance Plan	Draft of Product Assurance Plan for the Correlator Upgrade
PMD-365-031-A-PLA	Safety Compliance Plan	Draft of Safety Plan for the Correlator Upgrade
PMD-365-032-A-PLA	Correlator Upgrade Specification	Detailed specifications of the upgraded correlator
PMD-365-033-A-REP	Recommended Hardware System Changes	Details the study group's view of changes required in the ALMA system hardware to accommodate the correlator upgrade
PMD-365-034-A-REP	Rack Clock Skew Test Report	

Document Number	Document Title	Description
PMD-365-035-A-PLA	Manufacturing Plan	How the various parts of the system will be manufactured
PMD-365-036-A-REP	Analysis of the Sensitivity Degradation in a Digital FXF Correlator	Effects of truncation in ALMA2 and at other points in the system
PMD-365-037-A-REP	System Cost Estimate	Estimate of hardware costs and personnel effort
PMD-365-038-A-PLA	Installation Plan	Details the approach to installation
PMD-365-039-A-REP	Recommended Software System Changes	Details the study group's view of changes required in the ALMA system software to accommodate the correlator upgrade

Appendix D – Curriculum Vitae of Key Personnel

Rodrigo Amestica

- **Affiliation:** National Radio Astronomy Observatory
- **Contact Info:** ramestica@nrao.edu 434-296-0230
- **Education:**
  - 1995: MSEE, University of Chile.
  - 1995: BSEE, University of Chile.
- **Work Experience:**
  - 2003-present: NRAO, NTC
    - ALMA Control and Correlator group lead deputy.
    - ALMA Correlator Data Processor lead developer. Distributed correlator data processing design, testing and integration.
  - 1996-2003: European Southern Observatory
    - Joint Software Group leader
    - Telescope Commissioning head's deputy at Paranal.
    - Telescope Control Software developer. Real time telescope tracking, and supporting services (enclosure, site monitor).
  - 1992-1996: Mineral and Metallurgical Research Center (Chile)
    - Principal researcher.
    - Developed and validated of an on-line simulator of mineral concentration processes.
    - Developed a system for on-line characterization of color and size of bubbles over a flotation cell.
    - Development of a coarse ore size distribution sensor system upon the feeding of a Semiautogenous mill.
- **Publications**
  - Amestica, R., Gustafsson, B., Marson, R., 2006. Time synchronization within the ALMA software infrastructure SPIE 25-31 May 2006. Orlando, USA.
  - Kern, J., Amestica, R., 2004. The ALMA Real Time Monitor and Control Bus ADASS XIV, October 2004. Pasadena California
  - Pisano, J. A., Amestica, R., Perez, J. 2004. ALMA correlator computer systems SPIE 21-25 June 2004. Glasgow, Scotland United Kingdom
  - Glindemann, A., et al. The VLTI -- A Status Report Publication: Interferometry for Optical Astronomy II. Edited by Wesley A. Traub. Proceedings of the SPIE, Volume 4838, pp. 89-100 (2003). Publication Date: 2/2003
  - S. Sandrock, R. Amestica, P. Duhoux, J. Navarrete, M. Sarazin; The VLT Astronomical Site Monitor: control, automation and data flow; SPIE 4009, 27-31 March 2000, Munich, Germany.

Ray Escoffier

- **Affiliation:** National Radio Astronomy Observatory (retired)
- **Contact Info**

  Ray Escoffier
  184 Willow Dr.
  Gretna, LA 70053
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  rescoffi@nrao.edu
- **Work Experience**
  - 31 years direct NRAO employment plus 10 years NRAO consultant
  - Major Design Projects:
    - Architect and lead engineer for the first VLA correlator
    - Architect and lead engineer for the first VLBA correlator
    - Architect and lead engineer for the first GBT spectrometer
    - Architect and lead engineer for 64-Antenna ALMA Correlator
- **Managerial Experience:** Group Leader, NTC Correlator Group
- **Education**
  - BS in electrical engineering from LSU 1963
  - MS in electrical engineering from LSU 1967
- **Publications**
  - The ALMA Correlator, Astronomy and Astrophysics. September 2006

Joseph Greenberg

- **Affiliation:** NRAO NTC
- **Contact Info:** jgreenbe@nrao.edu 434-296-6366
- **Work Experience:**
  - NRAO
    - 1999-present: Design, build, install and upgrade ALMA Correlator
    - 1992-1998 Install VLBA Correlator in Socorro
    - 1985-1992 Design and build VLBA Correlator at NTC
    - 1971-1974 Co-op Student
  - 1979-1985:Boeing Commercial Airplane Company
    - Taught Maintenance Training of Commercial Airplane Avionics
  - 1975-1979:Honeywell Large Information Systems
    - Advanced Engineering Program
- **Education:**
  - BSEE: 1975 University of Cincinnati
  - MSEE: 1976 Arizona State University

Rich Lacasse

- **Affiliation:** NRAO NTC
- **Contact Info:** rlacasse@nrao.edu 434-296-0258
- **Work Experience:**
  - 2006 - present :NRAO, NTC:
    - ALMA Correlator: Design, manage (group and IPT leader) and test
    - ALMA Phasing Project NRAO lead engineer, system and FPGA design
  - 1976 – 2006: NRAO, Green Bank
    - Responsibilities
      - Electronics Division Head, four years
      - Digital Group Leader, many years
      - Telescope equipment trouble-shooting and maintenance
      - VLBI engineer (configure and test observing config)
    - Larger design projects
      - GBT Active Surface: servo design, p/o hardware and software design
      - GBT servo systems(AZ/EL, prime and secondary focus): liason with manufacturer, test configuration and witness
      - Spectral Processor: p/o architecture and digital/analog design
      - MKIII VLBI system: design of total power integrator
  - 1984 – 1985: CSIRO Division of Radiophysics
    - Design of digital delay for the AT Correlator
  - Charles Stark Draper Laboratories, Cambridge, MA
    - Design of circuitry used in missile guidance, mostly high-speed servo systems and Analog to Digital converters.
- **Education**:
  - 1974: MSEE, Stanford University, Stanford, CA
  - 1973: BSEE, Merrimack College, No. Andover, MA (4.00/4.00 GPA)
- **Publications**:
  - The Green Bank Telescope Pulsar Spigot, ADS Bibcode: 2005PASP..117..643K (view in ADS),Journal: Publications of the Astronomical Society of the Pacific, 2005, KAPLAN, D. L.; ESCOFFIER, R. P.; LACASSE, R. J.; O'NEIL, K.; FORD, J. M.; RANSOM, S. M.; ANDERSON, S. B.; CORDES, J. M.; LAZIO, T. J. W.; KULKARNI, S. R.

  - Green Bank Telescope Active Surface System, ADS Bibcode:1998SPIE.3351..310L (view in ADS), Proc. SPIE Vol. 3351, p. 310-319, Telescope Control Systems III, Hilton Lewis; Ed., 1998, LACASSE, RICHARD J.

  - Very-long-baseline radio interferometry - The Mark III system for geodesy, astrometry, and aperture synthesis, ADS Bibcode: 1983Sci...219...51R (view in ADS), Science, 1983, ROGERS, A. E. E.;CAPPALLO, R.J., HINTEREGGER, H. F., LEVINE, J. I., NESMAN, E. F., WEBBER, J. C., WHITNEY, A. R., CLARK, T. A., MA, C., RYAN, J., COREY, B. E., COUNSELMAN, C. C., HERRING, T. A., SHAPIRO, I. I., KNIGHT, C. A., SHAFFER, D. B., VANDENBERG, N. R., LACASSE, R., MAUZY, R., RAYHRER, B., SCHUPLER, B. R., PIGG, J. C.

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- **Work Experience:**
  - 2008 - present :ALMA, Chile
    - Correlator Group Leader
    - Commissioning of both the baseline and ACA correlators
    - Support of correlator and data transmission system
    - Support of software development efforts
    - Design team for ALMA Phasing project
  - 2005 – 2007
    - NRAO, NTC
      - Firmware, FPGA and system test design for ALMA Correlator
      - Commissioning of baseline and 2-Antenna correlators
  - 2004: DATANET: embedded system design
  - 1999 – 2004: Universidad de Chile: Research Engineer
    - Various Laboratory and Research Assistant position
  - 2003: Institut National Polytechnique de Grenoble, France
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- **Education**
  - Universidad de Chile: BSEE
- **Publications**
  - "Performance Highlights of the ALMA Correlators" , SPIE 2012
  - "Development of the Testing Interferometer for ALMA" , SPIE 2012
  - "On using ROACH2 as a daughter card", presented at 2013 CASPER workshop.
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  - "Monitoring temperature in FPGA based SoCs," 2005 International Conference on Computer Design, 634-637
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  - In summary: >10000 citations, >50 journal publications, 6 book sections, 20 invited talks and tutorials, 4 best paper awards, >100 conference contributions, 7 patents, 8 Master Theses, 8 Doctoral Dissertations h-index: 45, i10-index=111 http://scholar.google.com/citations?hl=en&user=5DLZvlMAAAAJ

Appendix E – Test and Installation Plan

The correlator upgrade team includes a significant number of members of the team who designed the current ALMA 64-Antenna Correlator. A great deal of experience was gained during the test and installation of that system. The current team plans to take advantage of that experience.

A significant difference between the installation of the current correlator and the installation of a new correlator is that ALMA is now a functioning observatory. There is a great demand for telescope time. Therefore, the previous successful approach to installation has been made more conservative to assure that telescope downtime will be held to a minimum. The approach is detailed in the following document which was generated during the ALMA Correlator Upgrade Study Project

Introduction

The purpose of this report is to provide information on the production and installation of components of the ALMA2 upgrade to the 64-antenna ALMA correlator. The purpose of this upgrade is to increase the correlator's operational bandwidth by a factor of two and increase its spectral resolution by a factor of eight.

The strategy used to realize this upgrade will be to retain as much of the existing correlator infrastructure and software as possible, design new digital logic cards (also a new ASIC) with the requisite capability, and replace existing cards within the existing correlator racks with these newly designed cards.

The hardware part of the upgrade project will follow a few conceptually simple steps:

- Design new logic cards and a new ASIC as required for the upgrade
- Contract vendor for ASIC procurement
- Contract vendor to perform PCB layout of new logic cards
- Contract vendor for fabrication and assembly of new PCBs
- Test new PCBs individually in various card test fixtures
- Test new PCBs together in a small simulated system in Charlottesville
- Integrate the hardware with the software
- Re-test a subset of the new PCBs in a small simulated system at the OSF with live antennas.
- Install new PCBs and other parts necessary in the actual system
- Test system to demonstrate operational status

The process can be reduced to four major operations; design, manufacture, test, and installation. This report concentrates on the last three of these items. Additionally, the "test" component in this report concentrates on hardware testing. The testing of prototype ASICs, PCBs, firmware and FPGA personalities are considered part of the design process. System Test is covered in [RD1].

Acronyms

A list of the acronyms used in this document is given below.

ALMA	Atacama Large Millimeter Array
AOS	Array Operation Site (of the ALMA Observatory)
ASIC	Application-Specific Integrated Circuit
BOM	Bill of Materials
CDP	Correlator Data Processor
DRX	Data Receiver (part of DTS below)
DTS	Data Transmission System
FA	Final Adder
FPGA	Field-programmable Gate Array
JAO	Joint ALMA Observatory
LTA	Long Term Accumulator
NRAO	National Radio Astronomy Observatory
PAS	Provisional Acceptance on-Site
RFQ	Request For Proposal
OSF	Operation Support Facility (in Chile)
PO	Purchase Order
TFB	Tunable Filter Board

Manufacture

The manufacture part of the upgrade project can be broken into:

- ASIC procurement
- PCB layout
- PCB assembly
- Test fixture assembly
- Individual PCB testing

The first three of these items will be vendor activities with NRAO overview to insure acceptable outcomes and the last two will be NRAO tasks. The last two of these items will be completed at NRAO.

ASIC procurement

During the upgrade study project, a survey of ASIC manufacturers was made and a list of possible vendors to supply the ALMA2 ASIC put together. Phone meetings and some plant visits were made to insure that each company on the list was capable of and interested in supplying the ASIC. Each was asked to provide budgetary cost and time estimates for the IC.

Once funding for the upgrade is available, it will be a simple process to issue a competitive RFQ for supply of the chip. The quotes will be evaluated from both from technical and business perspectives. After award of the contract, meetings between NRAO and the successful bidder will be held at key points in the design and production process. The procurement will culminate with the delivery of the tested ASICs.

PCB Layout and PCB Assembly

These two activities are put together as a single activity because a single competitive RFQ for the two activities is contemplated. As with the ALMA2 ASIC, a company survey was made during the upgrade study project and a list of possible vendors made. As with the ASIC, phone and some plant visits were made and budgetary cost estimates requested.

Even though a single RFQ will be made for the two activities, the RFQ will request that separate and independent bids be submitted for layout and assembly to allow for the possibility of separate POs for the two items to minimize cost (e.g., layout and assembly contracts may go to different companies).

As with the ASIC RFQs, the PCB RFQs will be evaluated from both technical and business perspectives. After award of the contract(s), meetings between NRAO and the successful bidder(s) will be held at key points in the design and production process. For example, the layout process will require some iteration between NRAO and the successful bidder to optimize the layouts (items such as re-assigning FPGA pin-outs to reduce layout complexity).

The procurement of the PCB layout will culminate with the delivery of manufacturing files for the PCBs.

The procurement of the PCB assemblies will culminate with the delivery of assembled and visually inspected PCBs and a specified amount of spare components. The PCB vendor will supply all components except the ALMA2 ASICS. NRAO will perform the detailed electrical test of the PCBs. The PCB vendor will also supply "first-article" PCBs to NRAO for NRAO test and inspection prior to completing the manufacturing of the balance of the deliverables.

Testing

NRAO will design and construct test fixtures for all hardware testing. NRAO will perform all tests of completed assemblies and the completed system.

Test Fixture Assemblies

The upgrade project will require construction of three new test fixtures:

- A new DTS simulator
- A Correlator Card/FA test fixture
- A system test fixture

These test fixtures will be NRAO-built. Their functions and purposes are described in the following sections. Existing test fixtures will also be adapted for some of the cards. Two fixtures of each type will be constructed. One will be delivered to the OSF with the system.

Individual PCB Testing

A set of test fixtures will be used to individually test all of the upgrade PCBs. The test fixtures consist of old fixtures used to test cards for the original system build plus new test fixtures specifically for the upgrade PCBs.

All PCBs will be tested per updated test procedures. Some effort to revise test fixture firmware will be required but should not constitute a major activity.

System Testing

To assure that individual PCBs work together correctly as a system, two levels of system testing are envisioned. The system test fixture mentioned above handles the first level of system testing. This test fixture will consist of four racks: a power supply rack, a Station Rack, a Correlator Rack and a Computer Rack. The Station and Correlator racks will be very similar to those deployed at the AOS, both mechanically and electrically. This will assure that boards tested in this fixture will function correctly in the existing correlator. NRAO will construct and test this fixture. It will be necessary for NRAO to procure PCBs and hardware used in the original correlator construction to build this fixture.

This fixture will serve three purposes. The first is design verification – to assure that the integrated design meets its requirements. The second is card burn-in. The production plan allows for about 2.5 weeks of burn-in time for each card that is to be delivered to Chile. The final purpose is hardware-software integration. This is to assure, to the greatest extent possible with a system this size, that the hardware and software will work together at the AOS and meet spec.

An anticipated parallel project dubbed "The Fifth Quadrant" and constructed by JAO, will result in the construction of a second System Test Fixture at the OSF. The fixture will be essentially identical to the system test fixture in Charlottesville. This fixture will be connected to live antennas and will be primarily used for software testing. The upgrade project plans to make use of this fixture as a final means of system test. A subset of the delivered cards will be installed in this system and tested with live antennas to provide additional assurance that operation in the correlator will be correct. It will be necessary to add LVDS cables to the fixture to connect the Correlator Cards to the Final Adders. These can be removed at the completion of the test if necessary.

Installation

The installation part of the upgrade project for this report consists of PCB installation into the correlator along with tests to verify that operation is correct. This will occur once all of the PCBs have been tested, both in individual test fixtures and in a simulated system environment. At this point in the project, there will be considerable confidence that the installation into the system at the AOS will be as problem-free as was the original correlator AOS installation.

All installation activities will be performed by NRAO.

In addition to PCB swaps, some new cables will have to be added to the system.

Swap-out of PCBs and installation of cables will probably be done one rack at a time with each rack undergoing extensive testing before the next rack is updated. To facilitate this approach, the packaging of cards for shipment to the AOS would be organized by rack (a lesson learned from the installation of the current correlator). While the entire correlator quadrant must be off-line as modifications are made, this rack-by-rack approach should allow the shortest overall down time.

Once all modifications and engineering testing is complete, the correlator will be subjected to essentially the same PAS acceptance tests as the original system to insure that the system is ready for operational use.

References

RD1: PMD-365-032-A-PLA, System Test Plan.