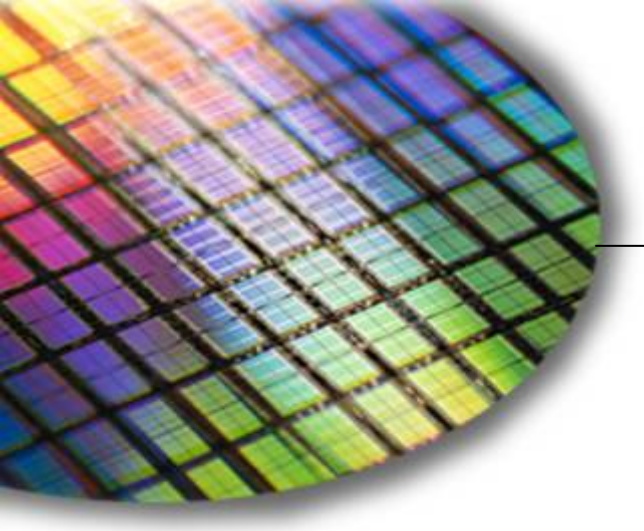

The World Leader in High Performance Signal Processing Solutions

Analog Devices, Inc.
Ultra Wideband ADC Technology Trends

Frank Murden

December 2015

ANALOG DEVICES

Topics

- CMOS Process Nodes
  - -Cost & Design Complexity
  - -Performance
- Innovation
  - -Pipeline ADC's
  - -CTSD
  - -SAR
  - -Interleaving
  - -Digital assistance
- Packaging
- Predictions for the Future

COST & DESIGN COMPLEXITY

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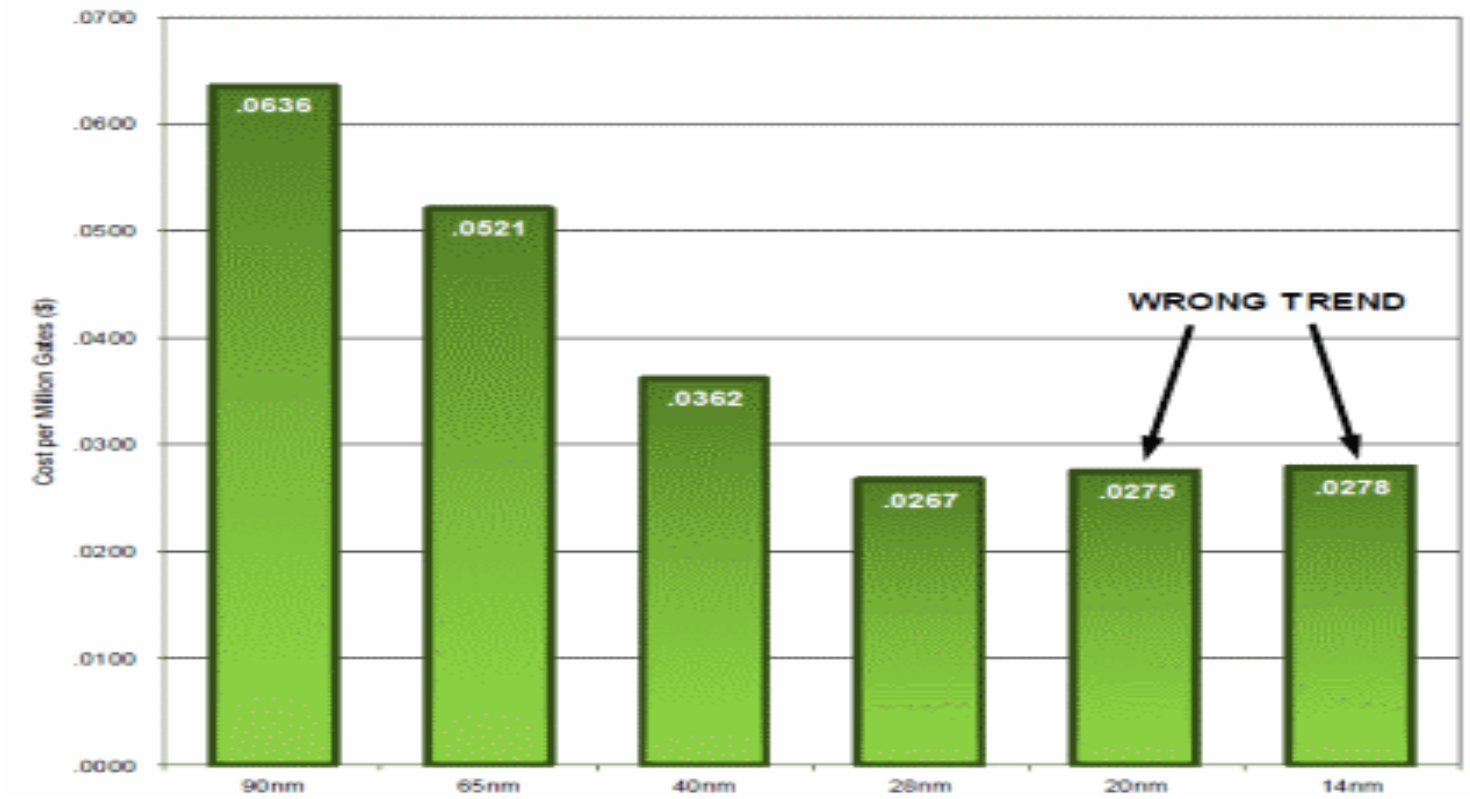
Industry Observation:

Improvements in cost/gate vs. process node ends below 28nm (has an impact on large digital engines)



- **Although Intel has made announcements that the trend may continue-TBD**

Source: H. Jones, "Feature dimension reduction slowdown", EETimes, 2012

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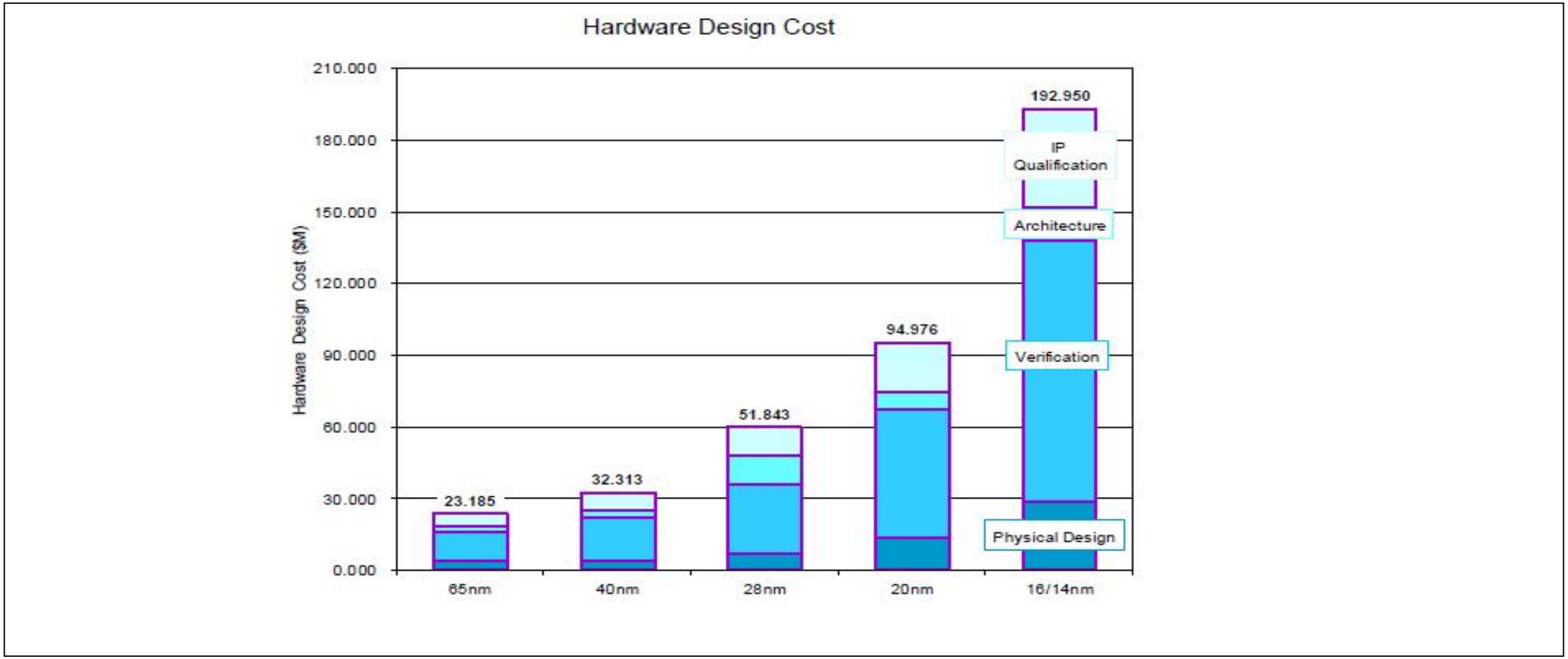
And complexity is driving rapid increases in the cost of design



Source: International Business Strategies, Inc 2013 report

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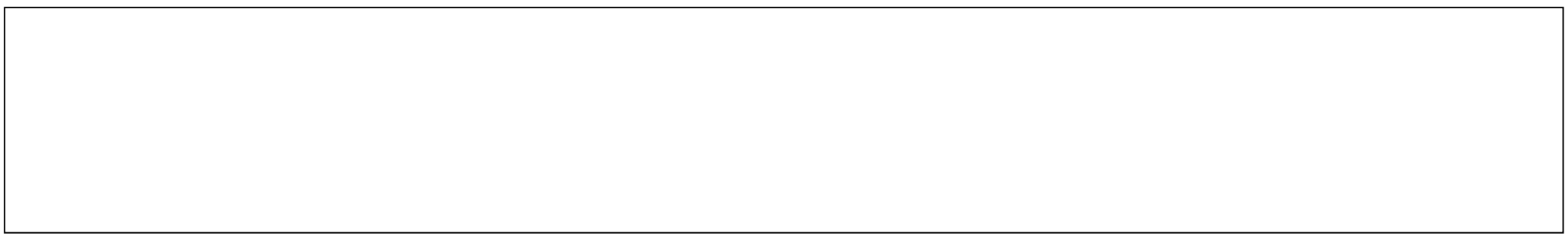

COMPARISON OF MASK SET COSTS TO REAL ESTATE IN THE NORTHEAST

180nm Mask Set
or
Nice ranch house in the Boston suburbs (New Hampshire)

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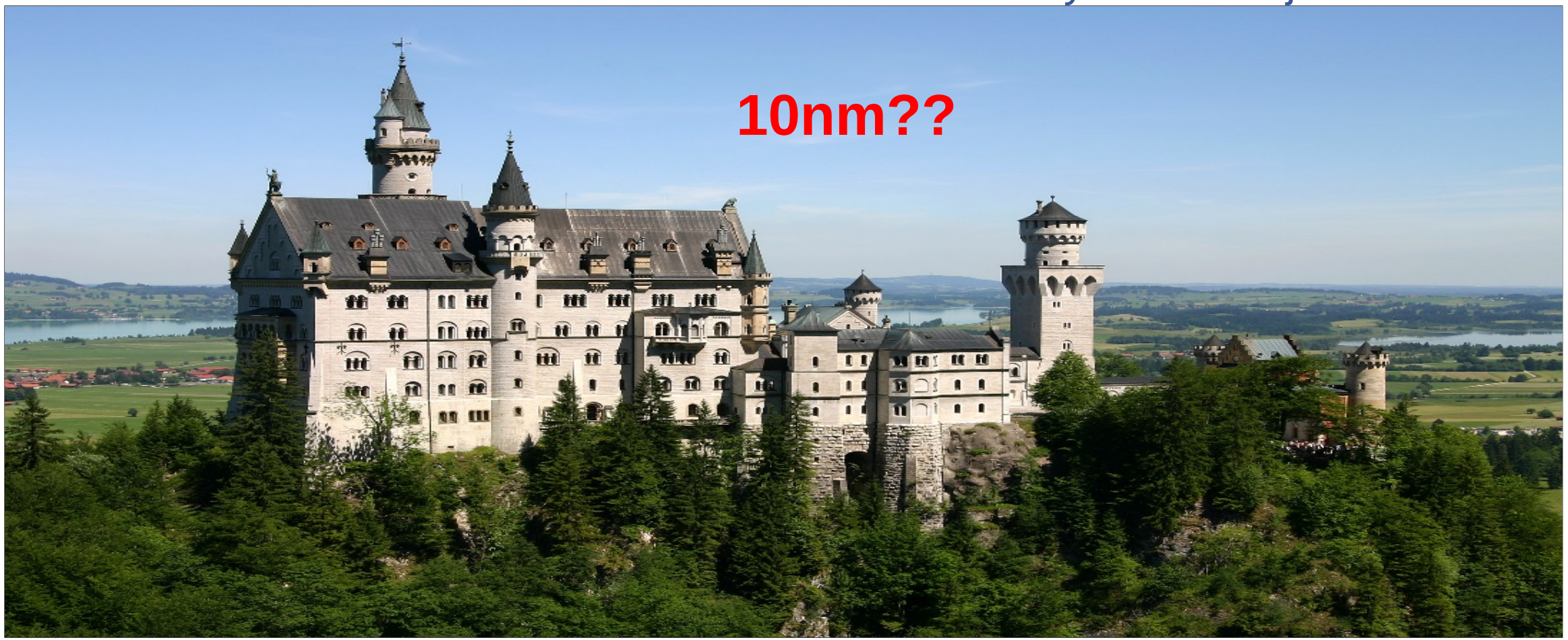
65nm Mask Set
or
Historic house in downtown Boston

28nm Mask Set
or
Eye-popping house in a classy Boston neighborhood

16nm Mask Set
or
Estate near the Boston waterfront

10nm Mask Set
or
Bavarian castle- commute to Boston in your Learjet



What's the take-away on process costs?

- **All aspects are increasing with decreasing feature size**
- **There are test chip shuttles to develop on to relieve initial mask set costs**

PROCESS NODE PERFORMANCE

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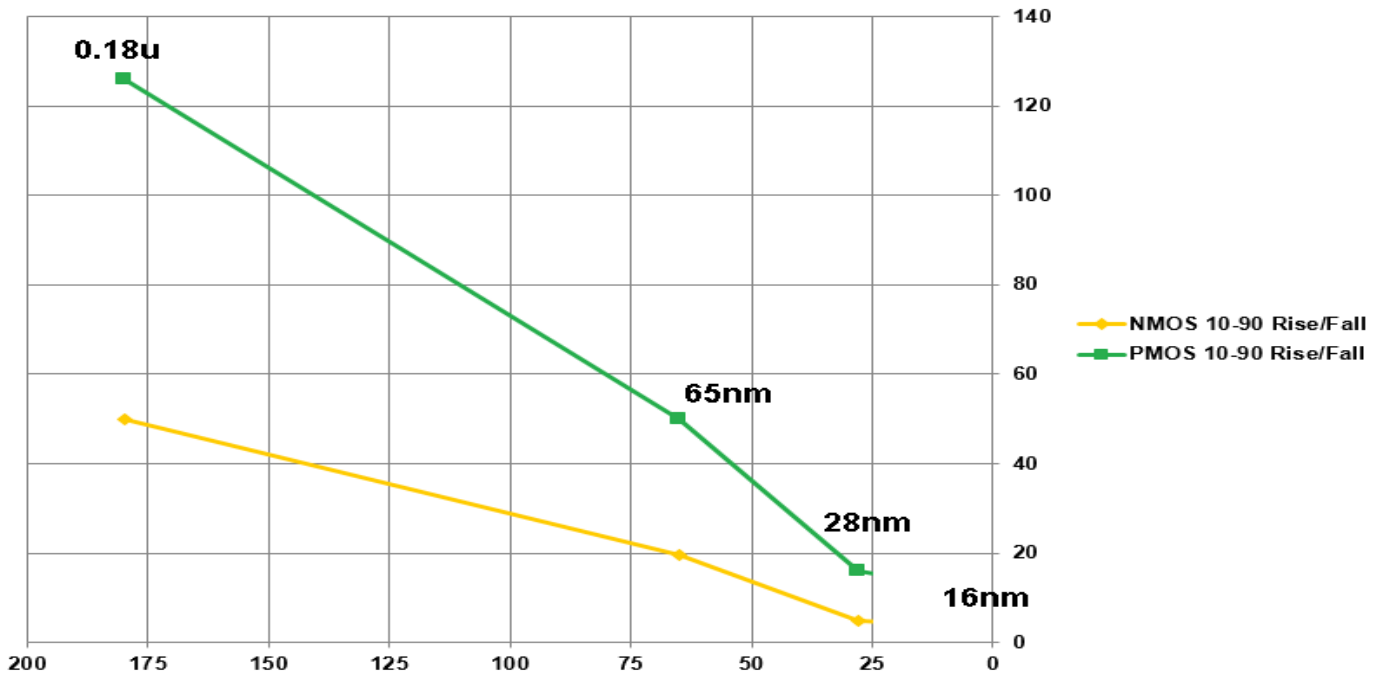
CMOS Rise/Fall Time vs. Process Node

(rise/fall time is a good marker of process analog performance)

- **A) Sampled time linearity is a function of rise/fall time (slew rate)**
- **B) Switch up-converted noise (jitter) is a function of rise/fall time (slew rate)**
- **What happens at 16nm and beyond?**



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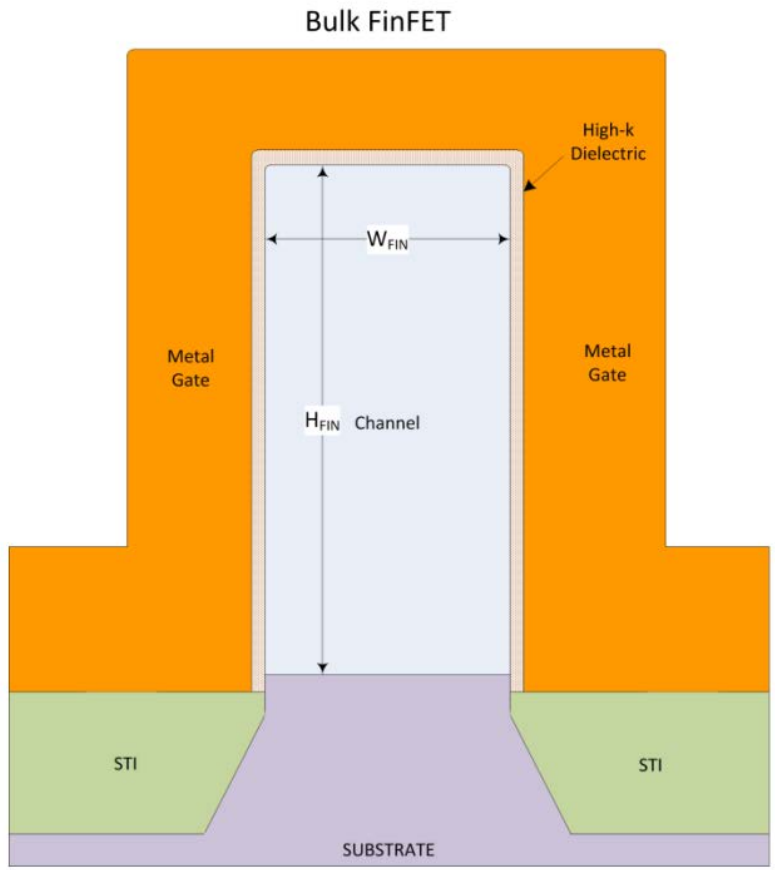
FinFET and Analog performance

- **FinFET is the only option beyond 20nm**
- **Planar transistor is history**

- **Analog performance**
  - **Substantially higher drain impedance and hence also higher intrinsic gain**
  - **Better V_T matching**
  - **Lower leakage**
  - **Higher device parasitics limit analog speed**

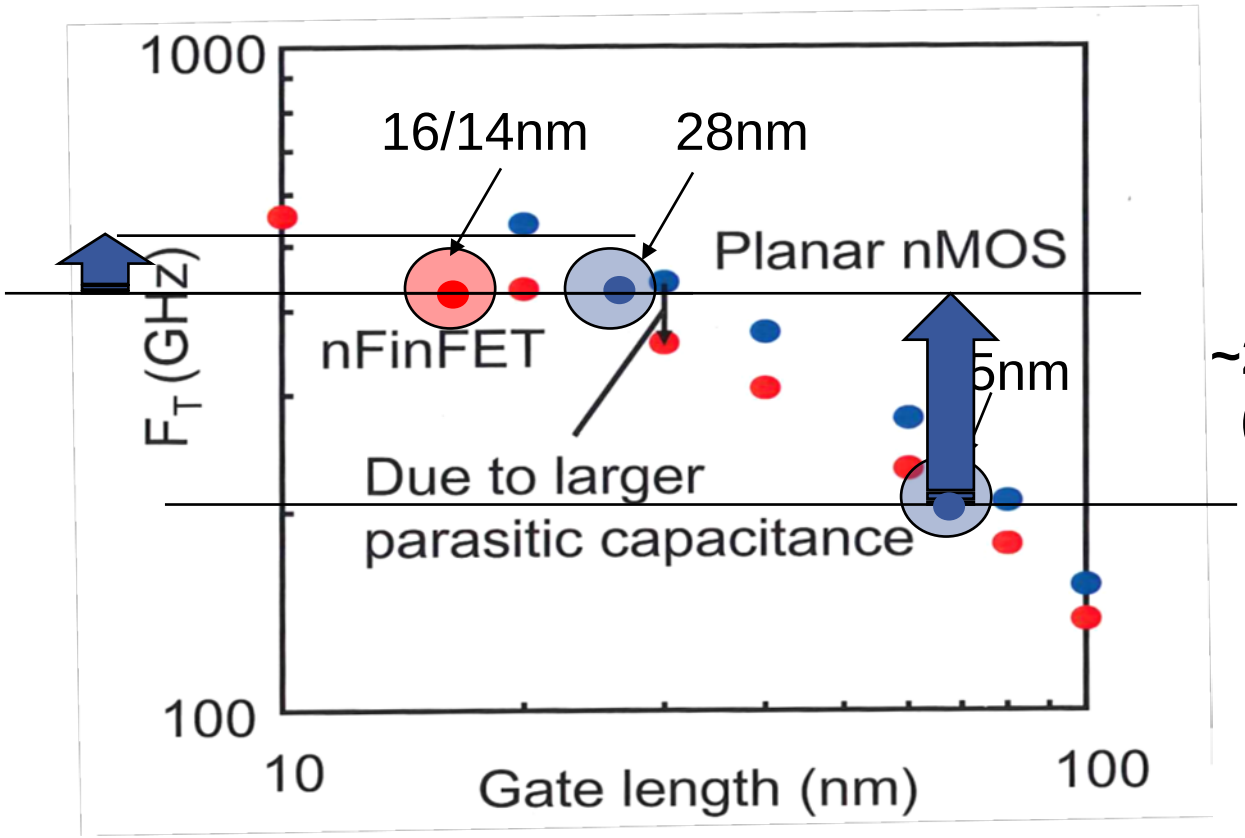
Main take-away: higher capacitance due to gate on three sides of the channel



Some content courtesy of T. Gaiser, Analog Devices, 2014

The issue is that FinFETs are intrinsically slower than planar FETs

~100GHz boost!
(~30% speed up)



~200GHz boost!
(2x speed up)

Would need to go to 8nm/10nm node to realize additional intrinsic f_T performance beyond 28nm

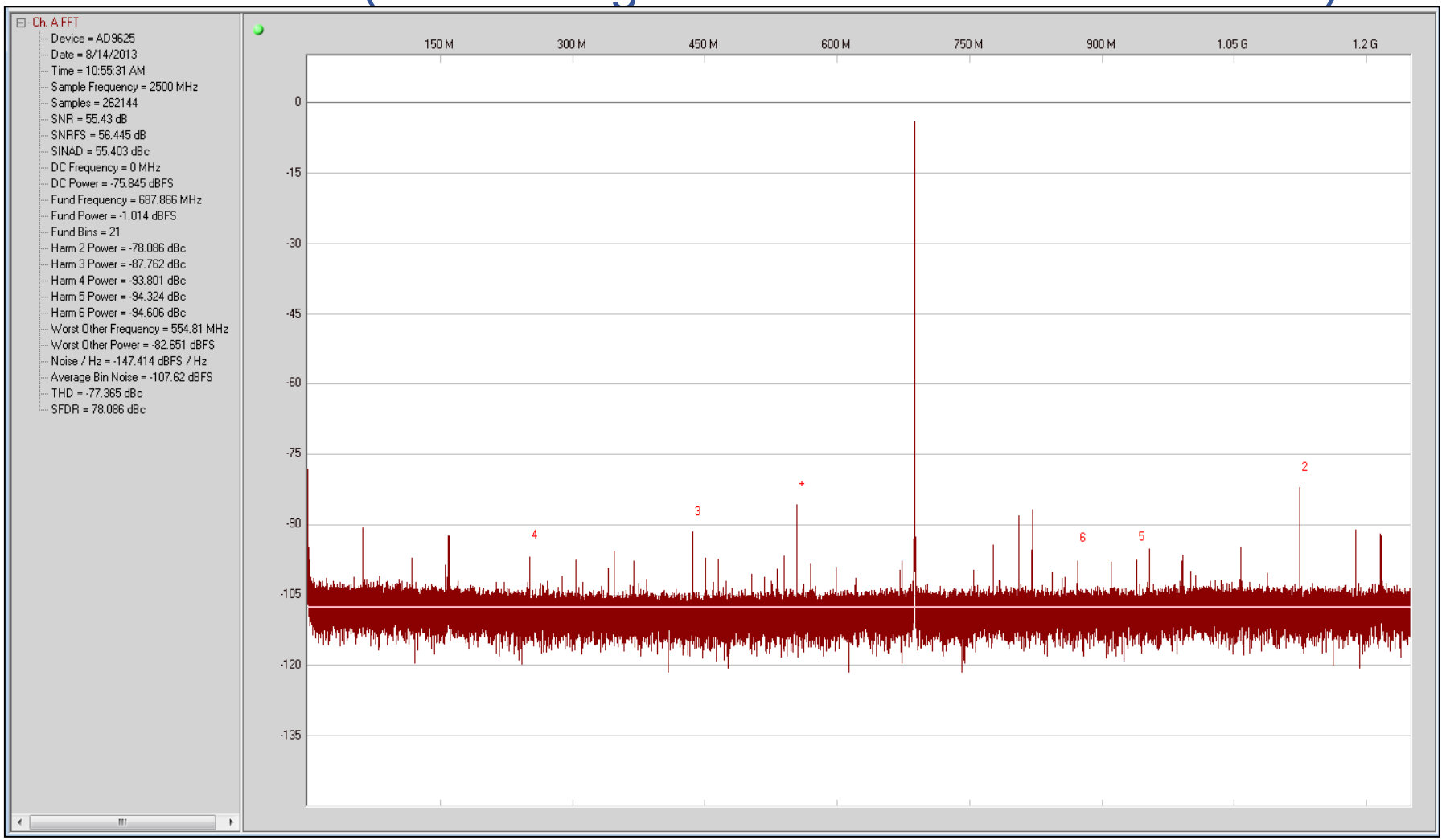
Source: T. Ohguro (Toshiba), "FinFET Technology for high-performance circuit design", Forum F1, ISSCC 2014

How Does that translate into ADC Performance?

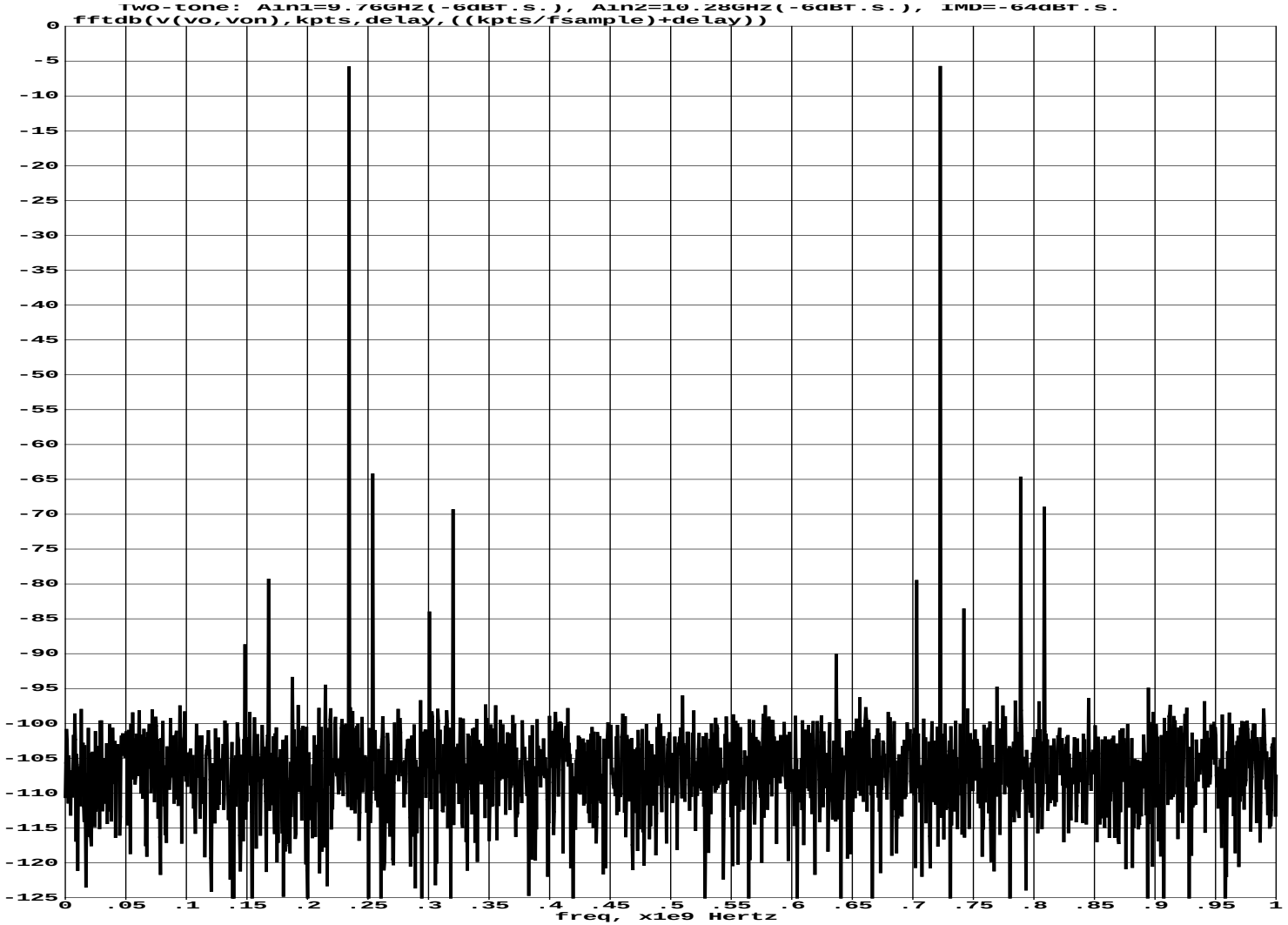
(Comparison of ADC Performance vs. CMOS Process Node)

- **180nm (2005)**
  - **(12-14)Bit (500 -> 250)MSPS**
  - **(-152 -> -156)dBfs/Hz ND**
  - **(-75 -> -80) dB to 400MHz Ain**
- **65nm (2010)- approximately 4-5x faster than 180nm node**
  - **(12-14)Bit (2500 -> 1250)MSPS**
  - **(-150 -> -156)dBfs/Hz ND**
  - **-75dB to 2GHz Ain**
- **28nm (2015)- approximately 2-2.5x faster than 65nm node**

AD9625 12B2.5GSPS (65nm process)
-1dB FS CW @ 1.8GHz, 3.8GHz BW
(small signal ND=-150dBfs/Hz ND)

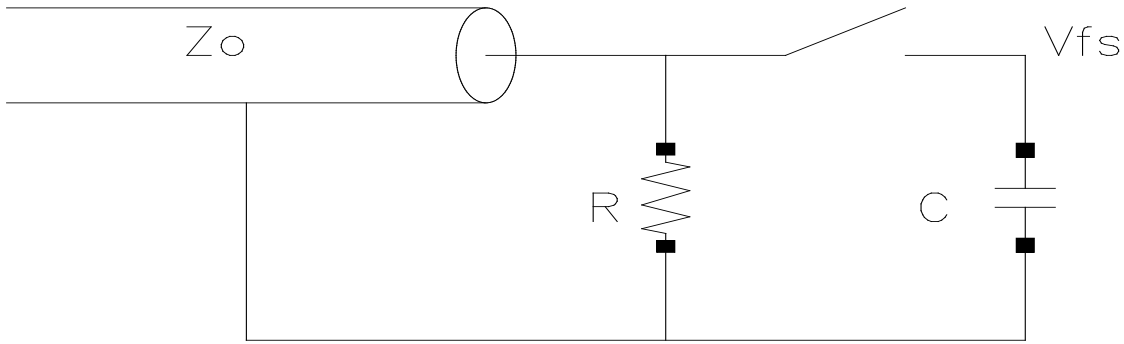


65nm (experimental concept, not a product)
Sampled Two Tone (9.76 & 10.28GHz) simulation, BW=18GHz, (small signal ND=-140dBfs/Hz)



ANALOG DEVICES

Which Brings us to the "Big Six" Performance Trade-offs of a Sampled System



- 1) $BW = \frac{2}{2\pi RC} = \frac{2}{2\pi ZoC}$ **2)** $\int noise = \sqrt{\frac{kT}{C}}$ **3)** $Pin = \frac{(0.5 * VfsRMS)^2}{R}$ 4) Sample Rate
- **5)** $Signal\ Linearity = vfs + k_2 {v_{fs}}^2 + k_3 {v_{fs}}^3$ 6) Power Dissipation

They are all a function of one another

“Big Six” make up a performance Box

- **The area of the sides or maybe the volume of the box is set by process and technical understanding**
- **The sides are the “Big Six”**
- **Example: If you increase SNR (by increasing capacitor size)**
- **-BW may decrease**
- **-Input power (Pin) may increase**
- **-Sample rate may decrease**
- **-Linearity may decrease**
- **-Power will likely go up**
-

INNOVATION

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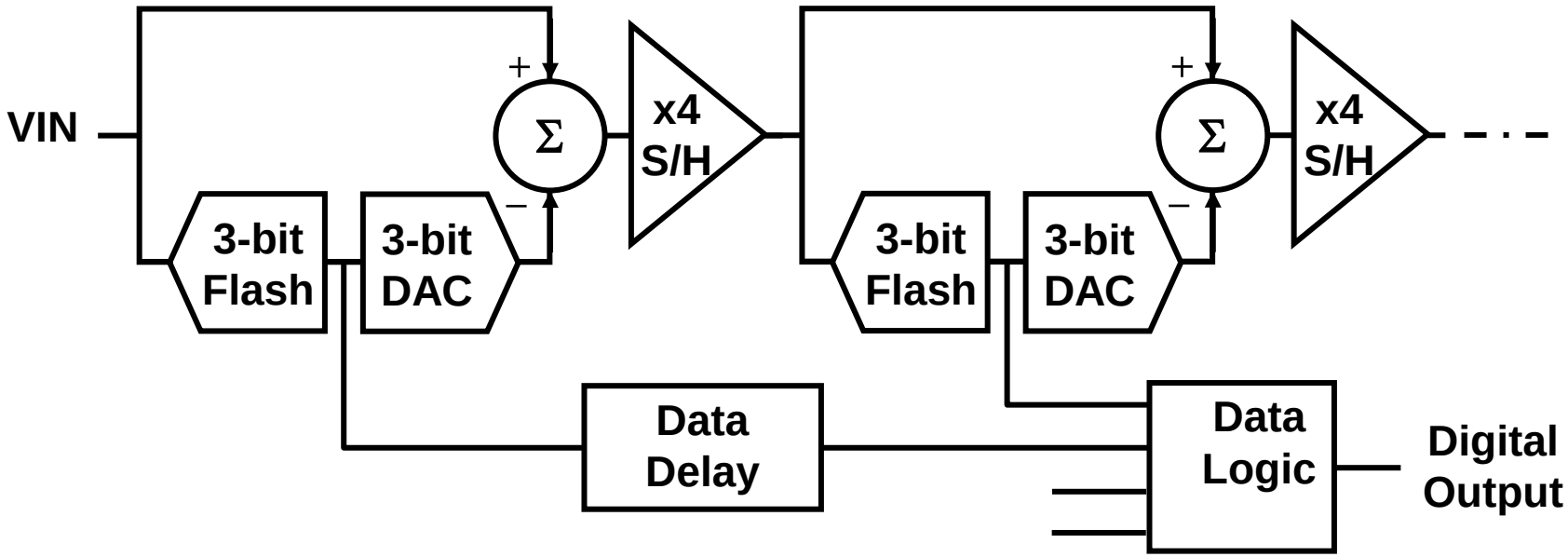
Pipelined Sub-ranging A/D

(high sample rate, high resolution "work-horse" architecture)



- **Sample Rate Determined by Speed of Stage 1 only**

•Continuous Improvements/Innovation (1000's of man-years) in all blocks have increased sample rate, SNR, linearity, reduced power

AD9680: Dual 14B 500/750/1000/1250MSPS 1.2/2.5V ADC (65nm process)

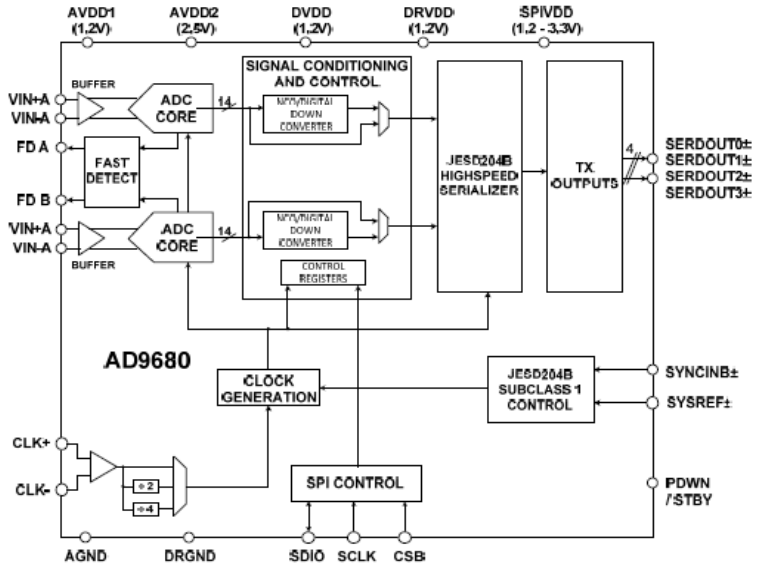
KEY BENEFITS

- **JESD204B (subclass 1) coded serial digital outputs**
  - **1.65W total power per channel at 1GSPS**
    - ***Noise Density = -154dBFs/Hz***
    - ***SFDR = 81 dBc at 340MHz Ain (1Gsps)***
    - ***SFDR = 78 dBc at 1000MHz Ain (1Gsps)***
    - ***ENOB = 10.9 bits***
- +/-0.5 LSB DNL, +/-1.0 LSB INL
- **Dual supplies : 1.2V and 2.5V/3.3V**
- Flexible Input range: 1.2Vp-p to 2Vp-p (1.6Vp-p nominal)
- **2G**Hz analog input bandwidth
- **>95dB channel isolation/crosstalk**

- **Amplitude detection for efficient AGC implementation**
- Two Integrated wide band digital down converters (DDC) per channel
  - **12-bit complex NCO**
  - 3 cascaded half band filters
  - Differential Clock input and divider
  - **Serial Port Control**
  - **Dither for improved signal linearity**
  - User-configurable, built-in self test (BIST)
  - **Energy-saving power-down modes**
  - Exportable version : **AD6674**

Key Benefit

- **High performance over wide bandwidth**



Temp	Package
-40°C – +85°C	64-LFCSP; Pb Free

Sampling	Final Release
Q1 2014	Q3 2014

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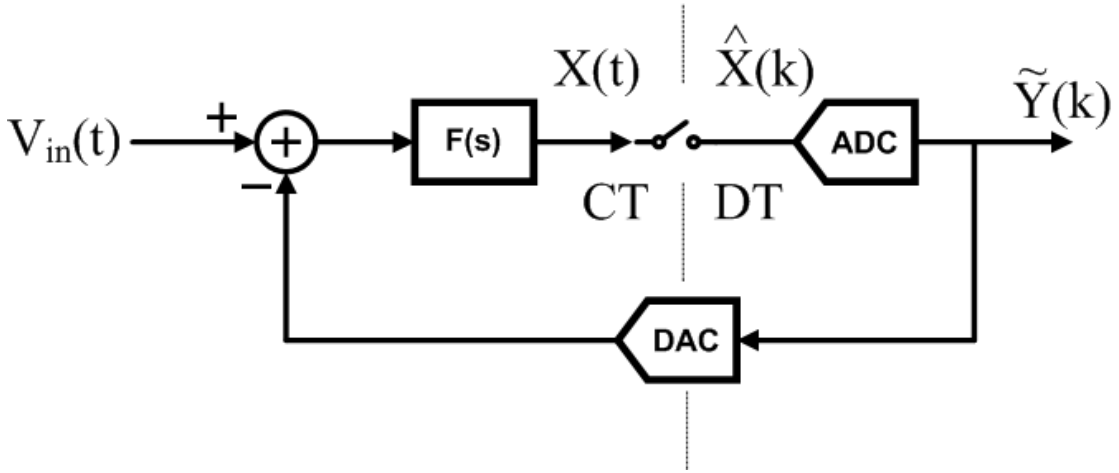
Continuous Time (CT) Δ-Σ modulator Architecture



- **Inherent anti-aliasing**
  - **Feedback system: X(t) is filtered by F(s) before being quantized and fed back**
  - **Elimination/simplification of the anti-aliasing filter triggers a "chain effect" in system simplification**
    - Remove lossy filters (e.g. SAW or crystal)
      - Remove driving amplifier (and its power and noise)
- **Resistive Input –easy to drive**

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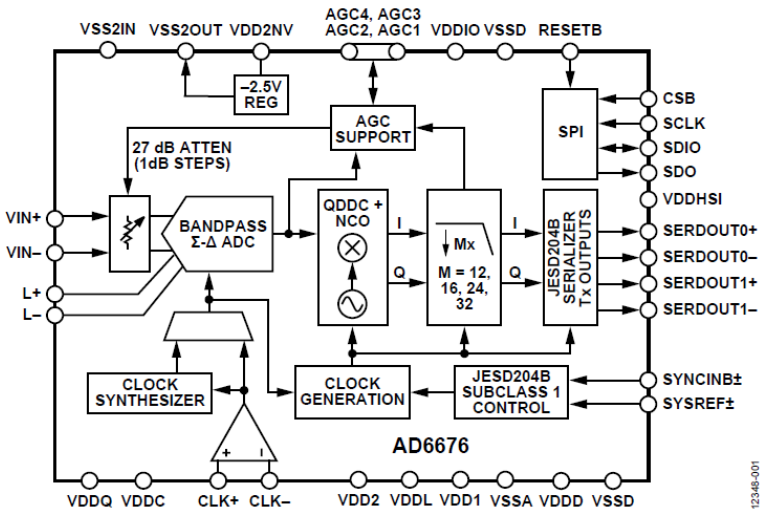
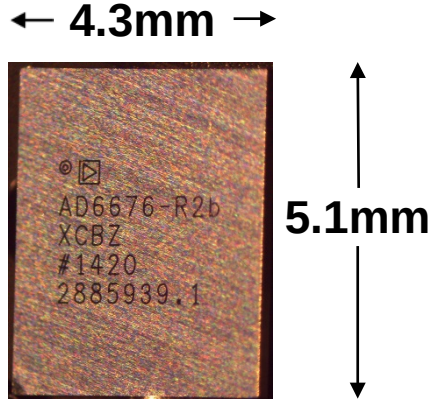
AD6676 Wideband IF Receiver Subsystem (65nm)

Enables Breakthrough Receiver Architectures

- **Industry leading Dynamic Range**
  - NSD of -159dBFS/Hz, IMD3 of -96dBc
  - IIP3 up to 36dBm, NF of 13dBm
- **Reconfigurable oversampled BP ΣΔ ADC technology**
  - Eliminates the need for SAW filter
  - BW to 150MHz
  - fo: DC to 1GHz
  - Very wide tunable IF receive platform
- **Simplifies ease of use**
  - Integrated PLL, Attenuator, DDC, JESD204B
  - Supports fast AGC control
  - Fast switching between different IF/BW profiles





http://www.analog.com/AD6676

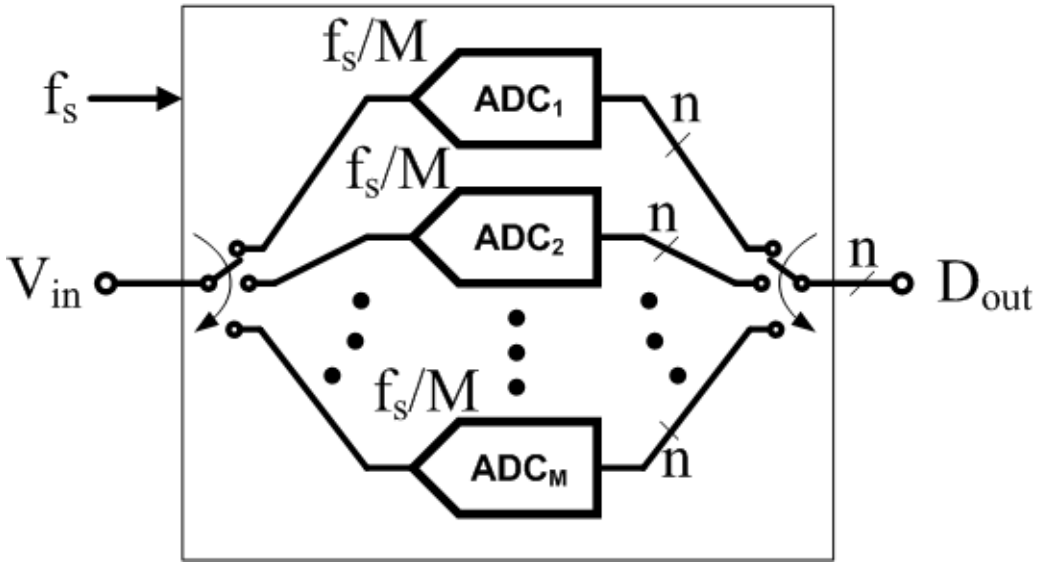
ANALOG DEVICES

IBM 8Bit 90GSPS ADC*

- 32nm SOI CMOS process (reduced S/D substrate capacitance)
- 8 bits
- 90GSPS
- 64x Interleaved SAR
- BW: 22GHz
- SNDR: 33dB SNDR up to 19.9GHz
- Power: 667mW (does not include digital output interface)

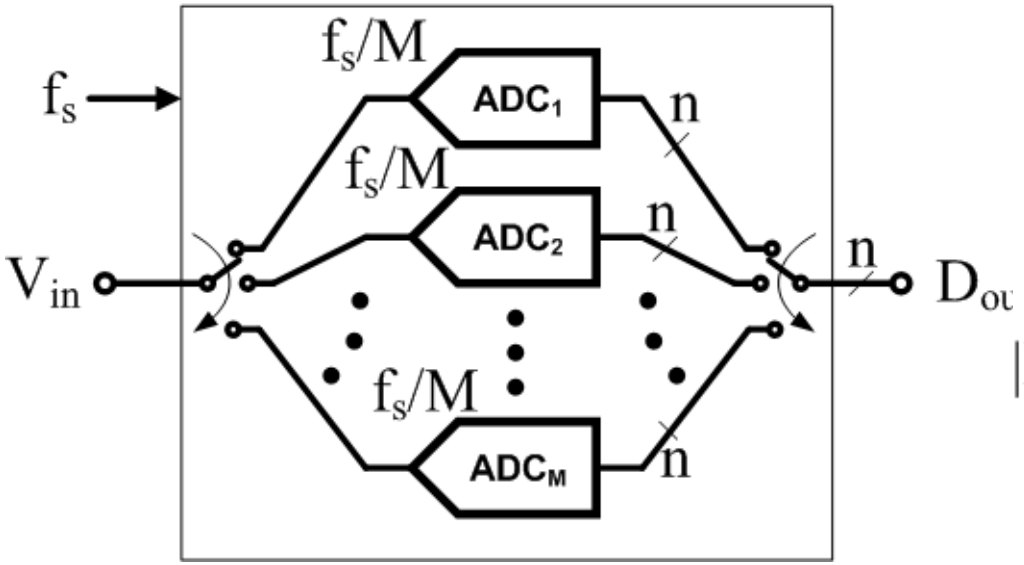
- *“A 90GS/s 8b 667mW 64× Interleaved SAR ADC in 32nm Digital SOI CMOS” by Lukas Kull, Thomas Toifl, Martin Schmatz, Pier Andrea Francese, Christian Menolfi, Matthias Braendli, Marcel Kossel, Thomas Morf, Toke Meyer Andersen, Yusuf Leblebici. International Solid-State Circuits Conference (ISSCC). Feb. 2014

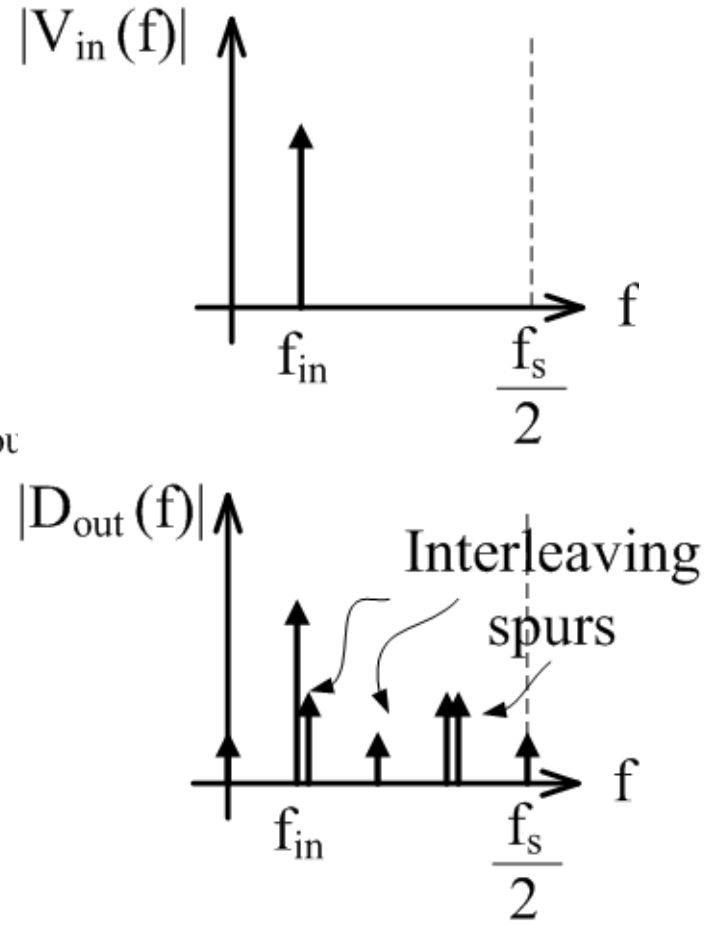
Time-interleaving: the basic idea
(Increase sample rate of a converter system)



- **Sample V_{in} with M identical converters in a round-robin (cyclic) fashion**
- **The sample rate of each converter is only f_s/M**
- **Power and area grow linearly with M**
- **Input BW ultimately becomes limited with excess M**

Time-interleaving: the reality- mismatches cause havoc





M=4 in this example

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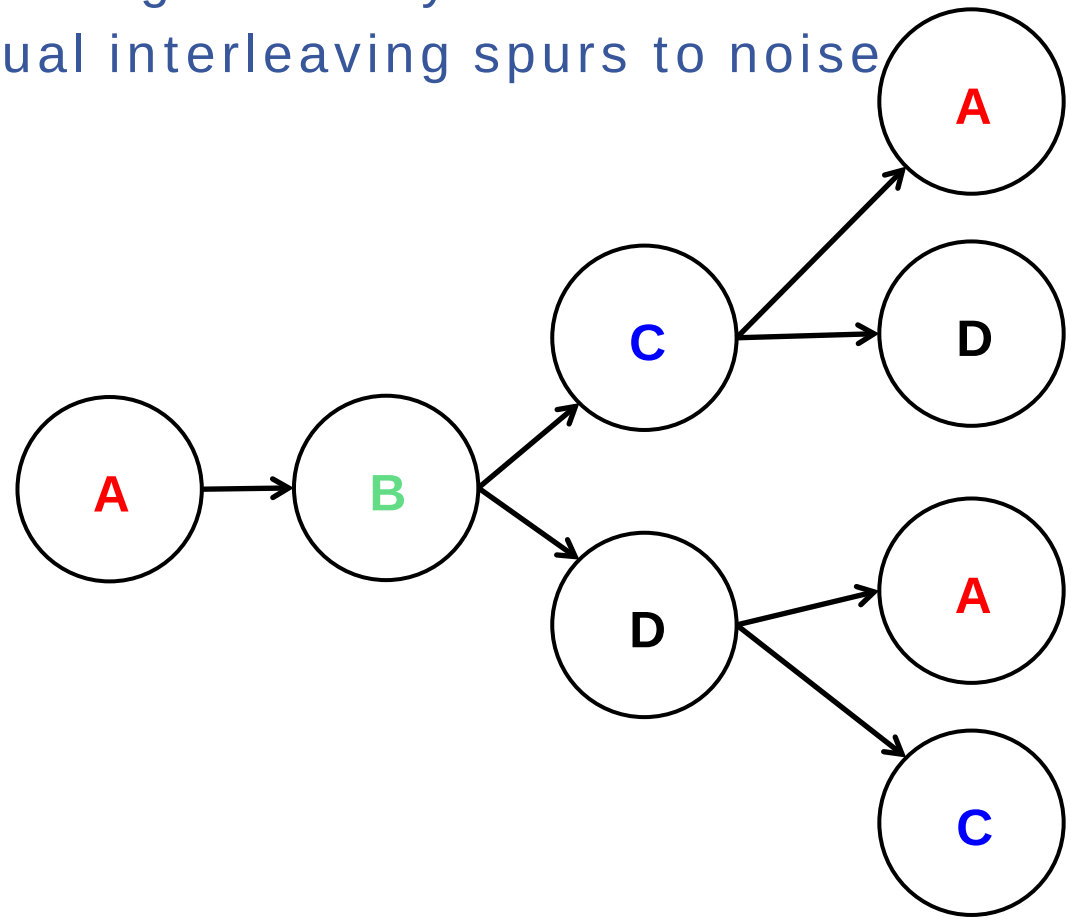
Time-interleaving: sub-ADCs mismatches

- **Offset error**
- **Gain error**
- **Sampling time skew**
- **Input bandwidth mismatch**
- **Multiple techniques can be used to “fix” impairments**

Interleaving and Shuffling Techniques

-reduce interleaving errors by trim or calibration

-convert residual interleaving spurs to noise



WHICH BRINGS US TO "DIGITALLY ASSISTED ANALOG"

“Digitally Assisted Analog” Calibration of A/D Converters

When Do You Correct?

- **Factory Calibration (fuses)**
- **Foreground Calibration (when ADC starts up)**
- **Background Calibration (while ADC is running)**

How Do You Correct?

- **Analog (or Mixed-Signal) Correction –”twiddle” analog functions**
- **Digital Pre/Post Correction- “twiddle” digital bits**

What Do You Correct?

- **DC Errors (mismatch, gain, offset)**
- **Timing Errors**
- **Dynamic Errors (e.g. distortion, incomplete settling, memory effects)**

Improve Power Efficiency, Speed, Dynamic Range, Integrate-ability

Packaging for High Performance ADC's

- CSP –chip scale packaging
- FCBGA –flip chip ball grid array
- Both styles allow for lower I/O inductance and controlled impedance vs. the "dangling/drooping" wire bond
- -CSP limited by minimum pad pitch
- -FCBGA allows for tighter ball pitch on die- redistribution layer "spreads"
- pitch to BGA
- -cost
- -additional impedance control of BGA/redistribution layer

WHERE IS ADC TECHNOLOGY HEADING?

Where is ADC Performance Heading?
Some basic observations

-28nm node is kind-of/sort-of 2-2.5X faster than 65nm

-16/14nm node kind-of/sort-of the same as the 28nm node (with better digital packing, leakage)

-In general ADC sample rate doubles, for the same power, resolution, linearity, on the same process node over subsequent generations due to innovation and process node understanding: Example: 12B250MSPS (180nm CMOS) => 12B500MSPS (180nmCMOS) same performance/power specs

-Interleaving improves sample rate but will ultimately start to limit BW from increased front-end parasitic loading.

-Power in the analog domain scales by the square with resolution:

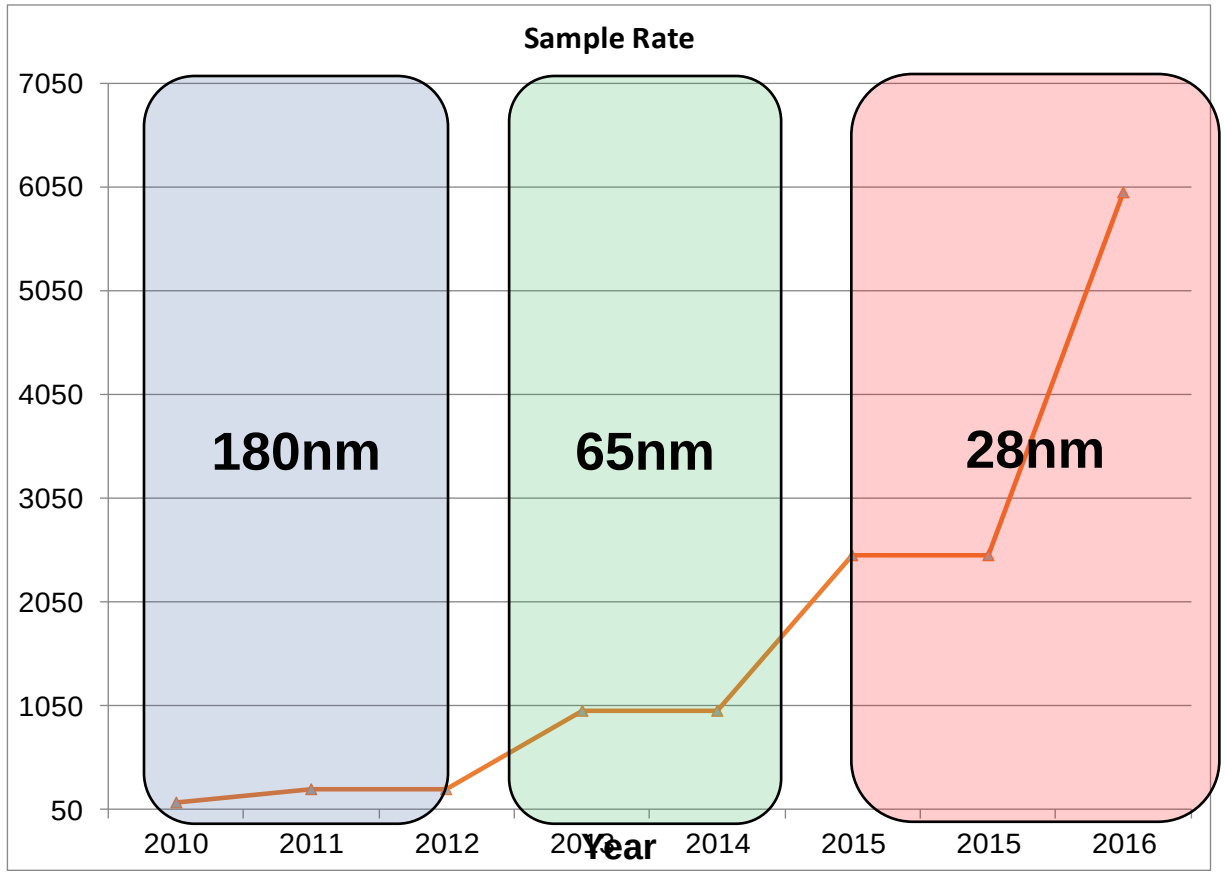
Example: 12 bits to 11 bits, analog power drops by ½

digital power only reduces slightly (11/12)

-The "Big Six" ultimately rules

Sample Rate Evolution of ADI's 14B pipeline ADC

(ND = -155 dBfs/Hz= -SNR -10log(fs/2))



-Keep noise density the same for increasing BW needs

-Process technology and architecture innovation drive the net gain.

Where is UWB ADC Performance Heading? Some possibilities as we head towards 2021

- **Very high sample rates at reduced resolution: Interleaving (data monster)**
- **Possible to achieve BW's as high as 1/10 f_T at reduced resolution (process, technology, & package advances)**
- **Increased linearity over frequency: "digitally assisted analog"**
- **Capability to achieve even higher sample rates and BW by moving to a smaller process node:**
-
- **"But this requires our CEO to sell his castle"**

THANK YOU

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