Integrated Digitization with Unformatted Serial Data Transfer

Matt Morgan

NGVLA Technical Workshop, Socorro, NM, December 8-9, 2015

Integrated Analog-Digital-Photonic Rcvr.
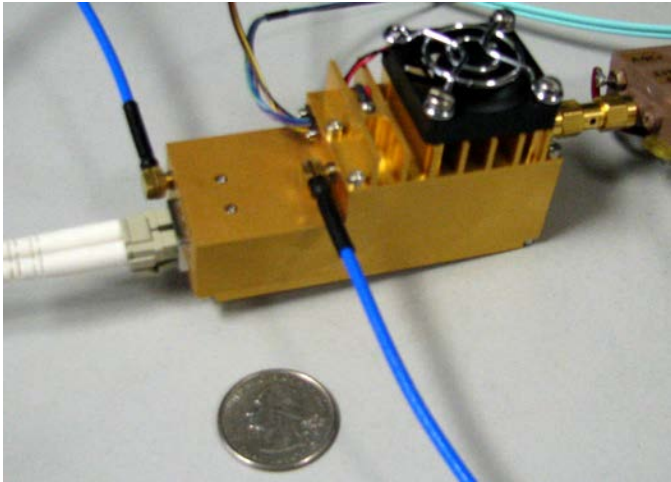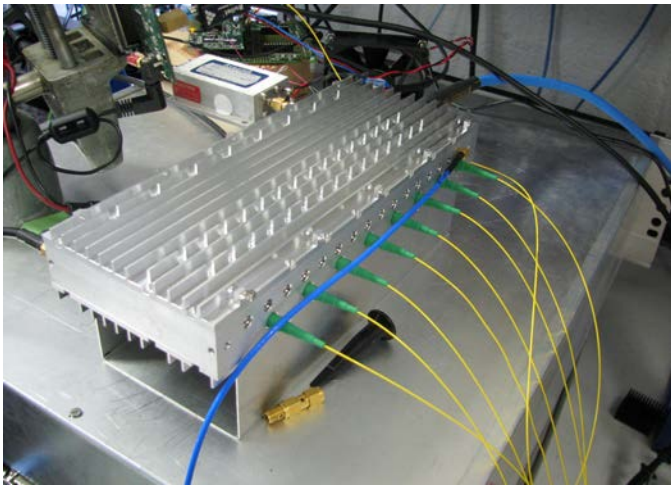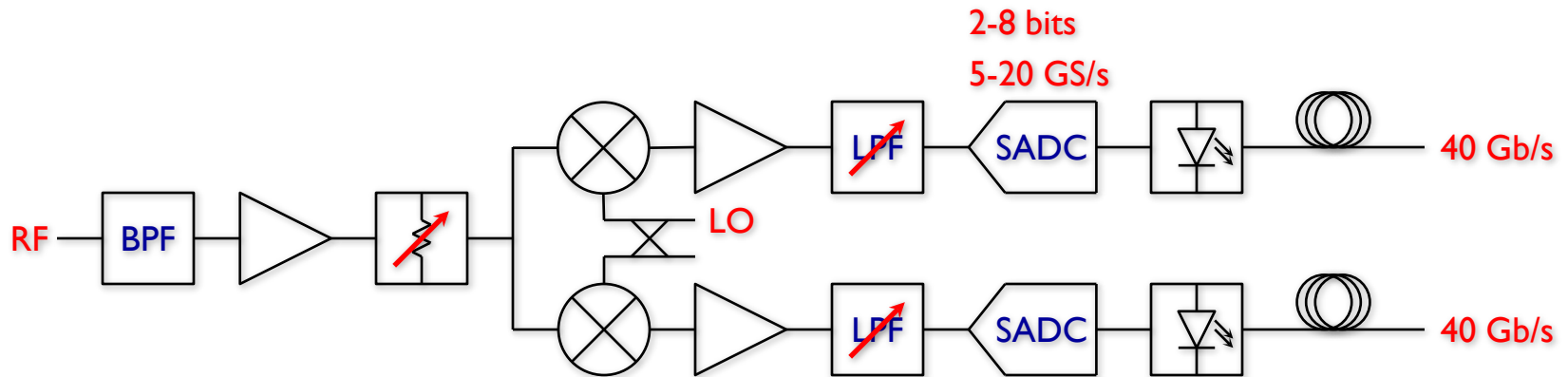

- Complete Warm-Electronics Package:
  - RF/IF amplification
  - Filtering
  - Power leveling
  - RF-to-baseband conversion
  - Analog-to-digital conversion
 - Copper-to-fiber conversion

- Operational Benefits:
  - Modular / Field-Replaceable
  - Mass and power consumption
  - Mean-Time-Between-Failures

High Frequency Module

- Single-stage, I/Q, direct-to-baseband downconversion
  - minimizes spurs
  - maximizes stability
- Integration also maximizes stability, uniformity, flatness

- 2-8 bit sampling (variable)
- 5-20 GS/s (aggregate 40 Gbps per IF channel)
- 1310nm, single-mode, low-optical power
  - "first mile" to long-distance backbone

Low-Frequency Module

Nyquist Zone Selection

2-8 bits
5-20 GS/s

RF — BPF — ▷ — ⚡ — BPF — ▷ — SADC — ▨ — ◎ — 40 Gb/s
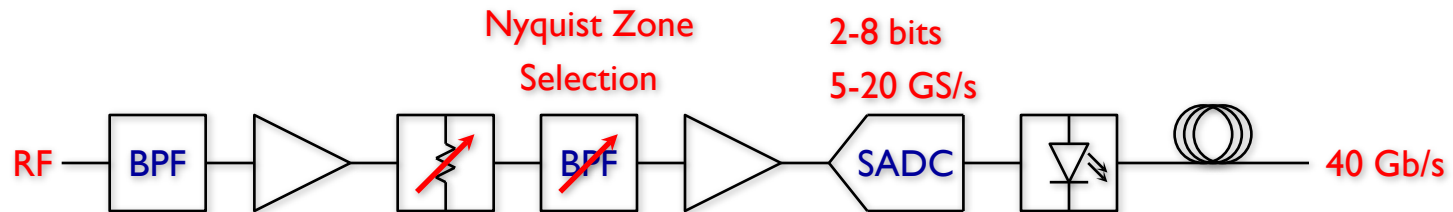
- Direct-Sampled
  - RF/IF Isolation
  - stability and uniformity

- Upper Nyquist zone and frequency to be determined

- 4-8 bit sampling (variable)

- 5-10 GS/s (aggregate 40 Gbps per IF channel)

- 1310nm, single-mode, low-optical power
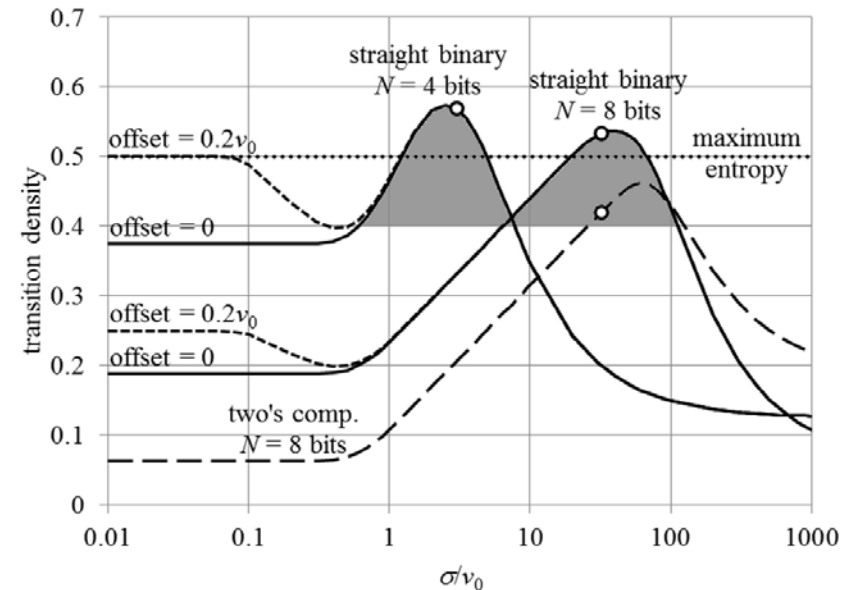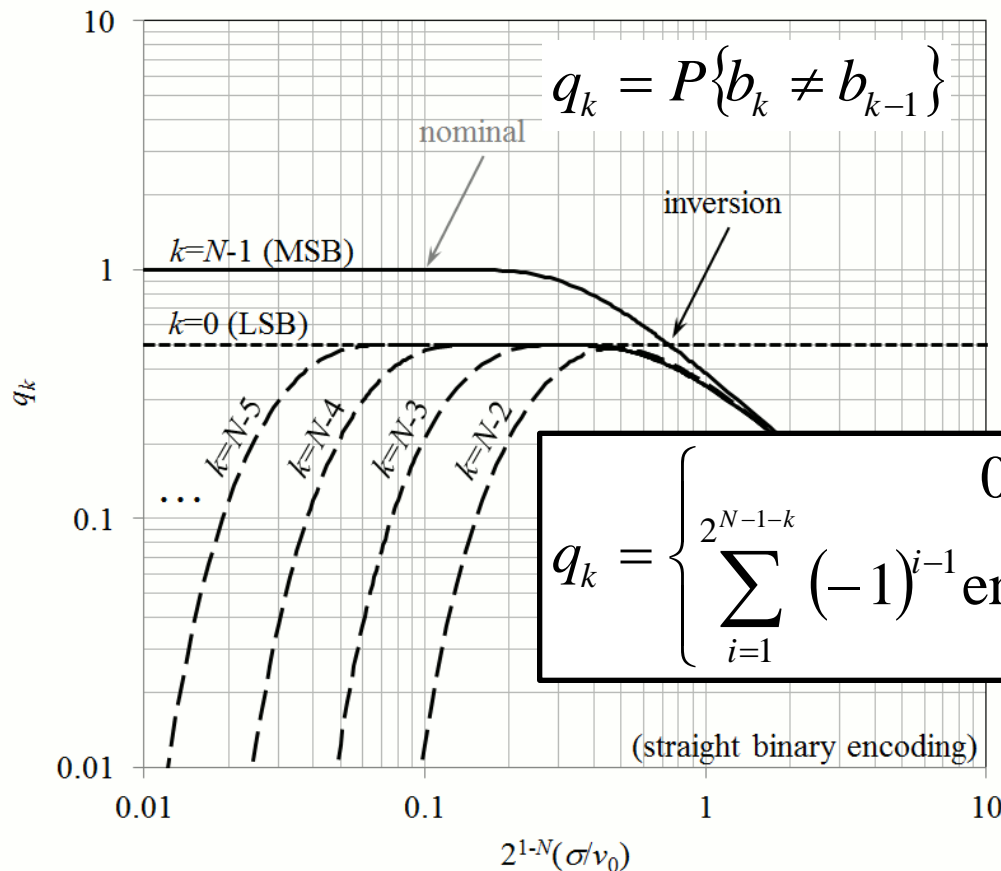 - "first mile" to long-distance backbone

Frequency Plan
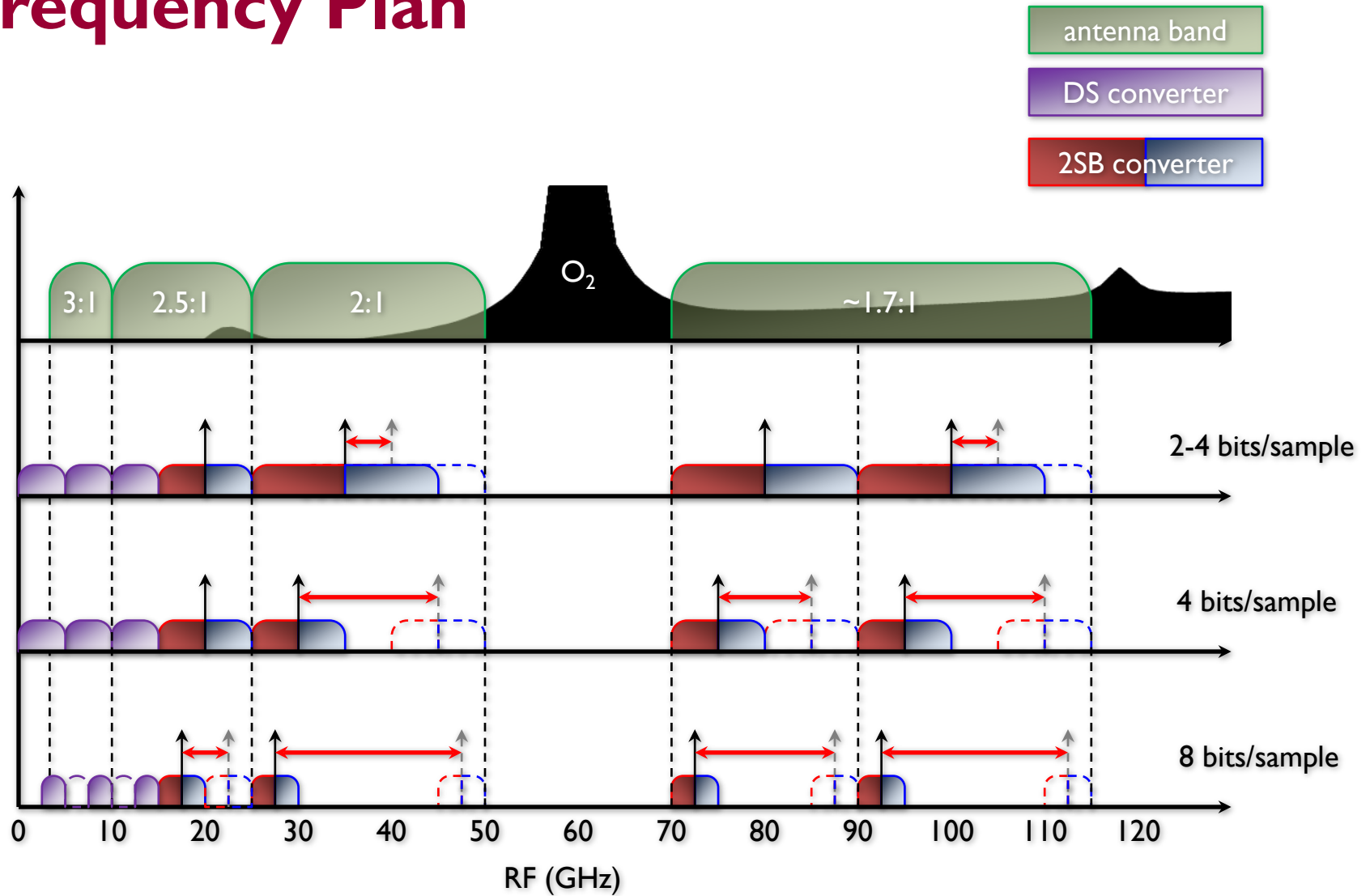
Unformatted Serial Link

Transition Density of Natural Signals

- Commercial deserializers can recover the clock from data streams that satisfy certain minimum transition density requirements.

- MAX3880 from Maxim IC:
  - "Tolerates >2000 Consecutive Identical Digits."

- VSC1236 from Vitesse:
  - signals Loss of Data when "transition density is less than 40%."
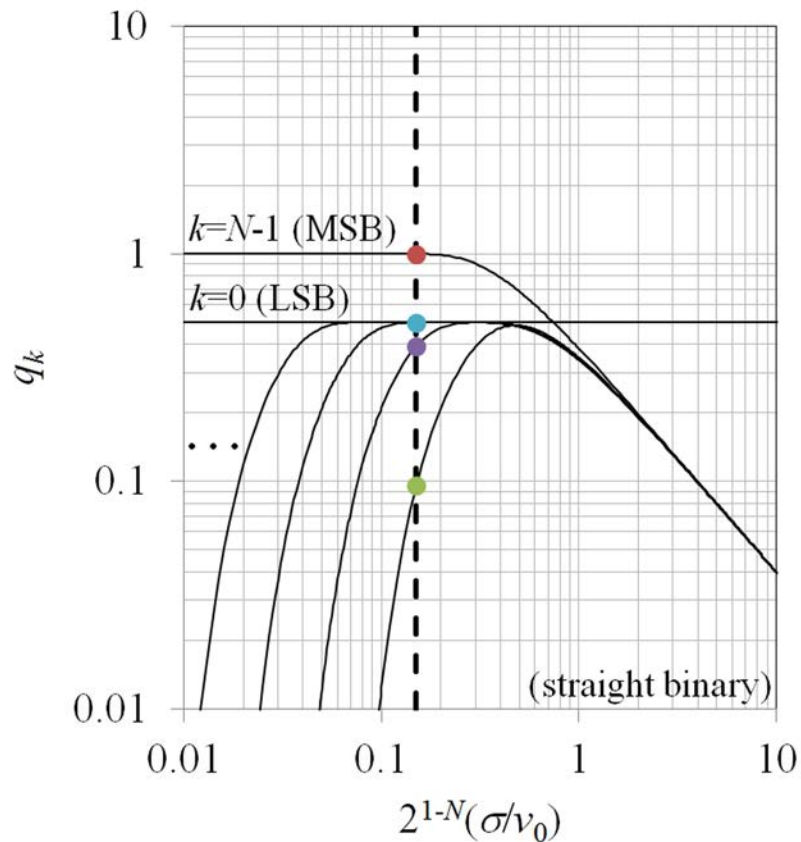
Word Alignment

$$q_k = P\{b_k \neq b_{k-1}\}$$

nominal

inversion

$k=N$-1 (MSB)

$k=0$ (LSB)

$k=N$-5 $k=N$-4 $k=N$-3 $k=N$-2

$$q_k = \begin{cases} 0.5 & k = 0 \\ 2\sum_{i=1}^{2^{N-1-k}} (-1)^{i-1} \mathrm{erf}\left(\frac{2^{N-1}-2^k\left(i-\frac{1}{2}\right)}{\sigma\sqrt{2}}v_0\right) & 1 \leq k < N \end{cases}$$

(straight binary encoding)

$2^{1-N}(\sigma/v_0)$

- The MSB has a predictable correlation with its neighboring bits in the most likely sample codes near the middle of the sampler range.
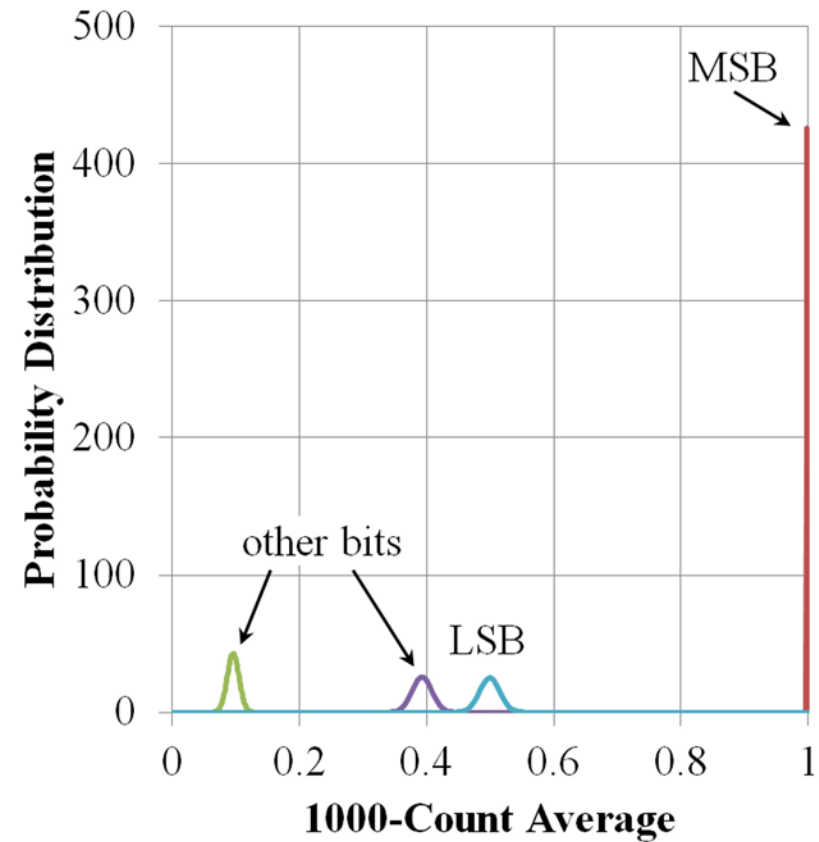
...ect ...n ...a serial data stream without any prior formatting.
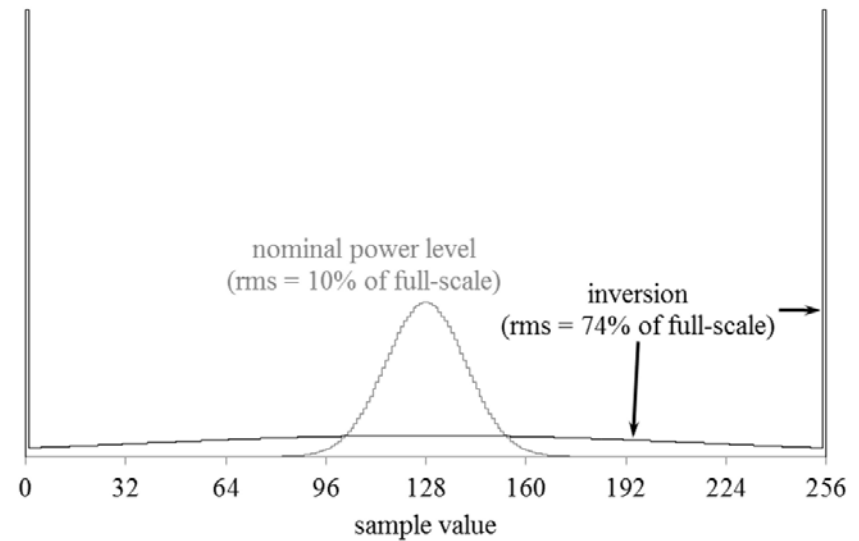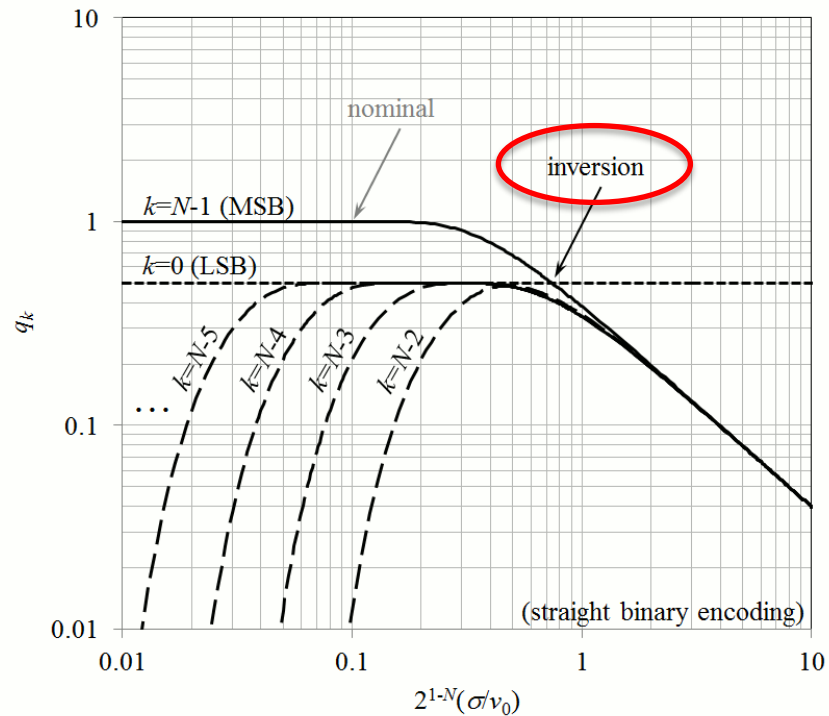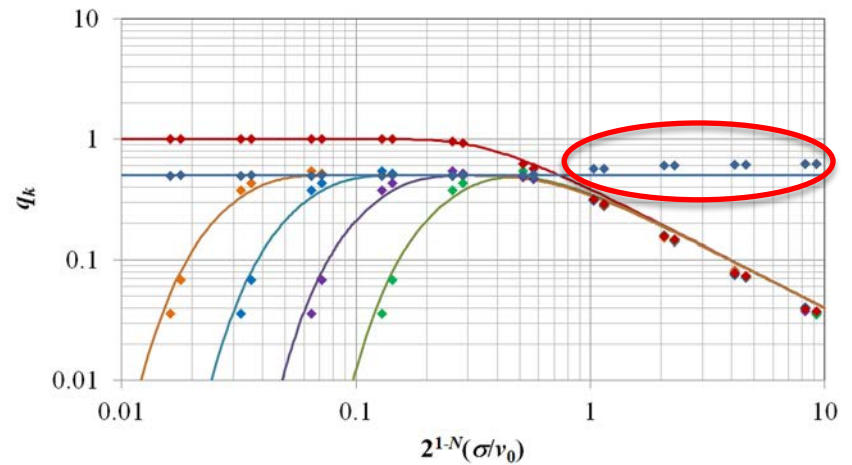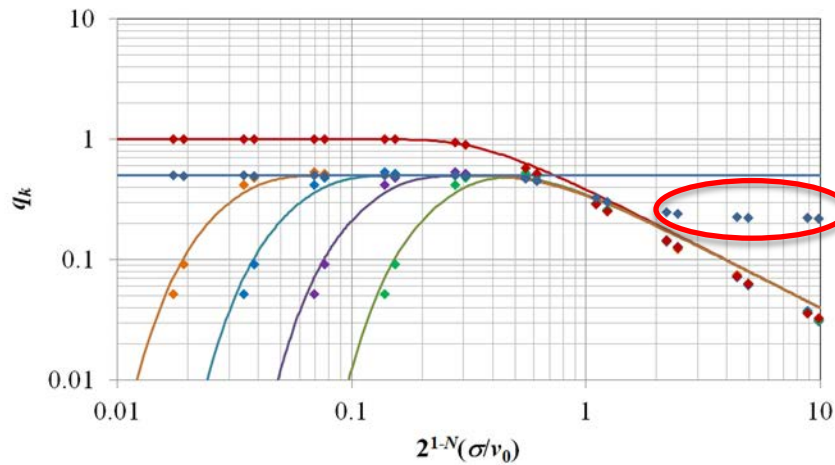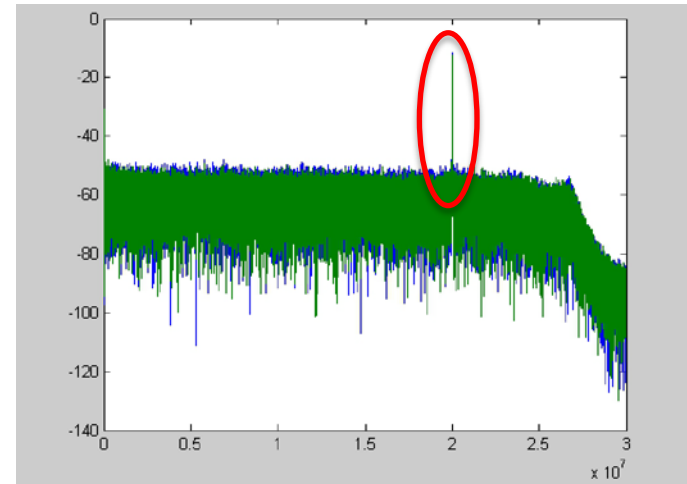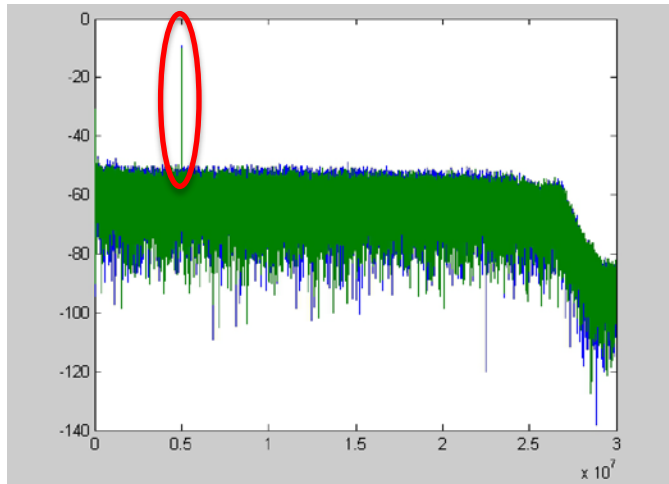
Scoring Probability Distribution
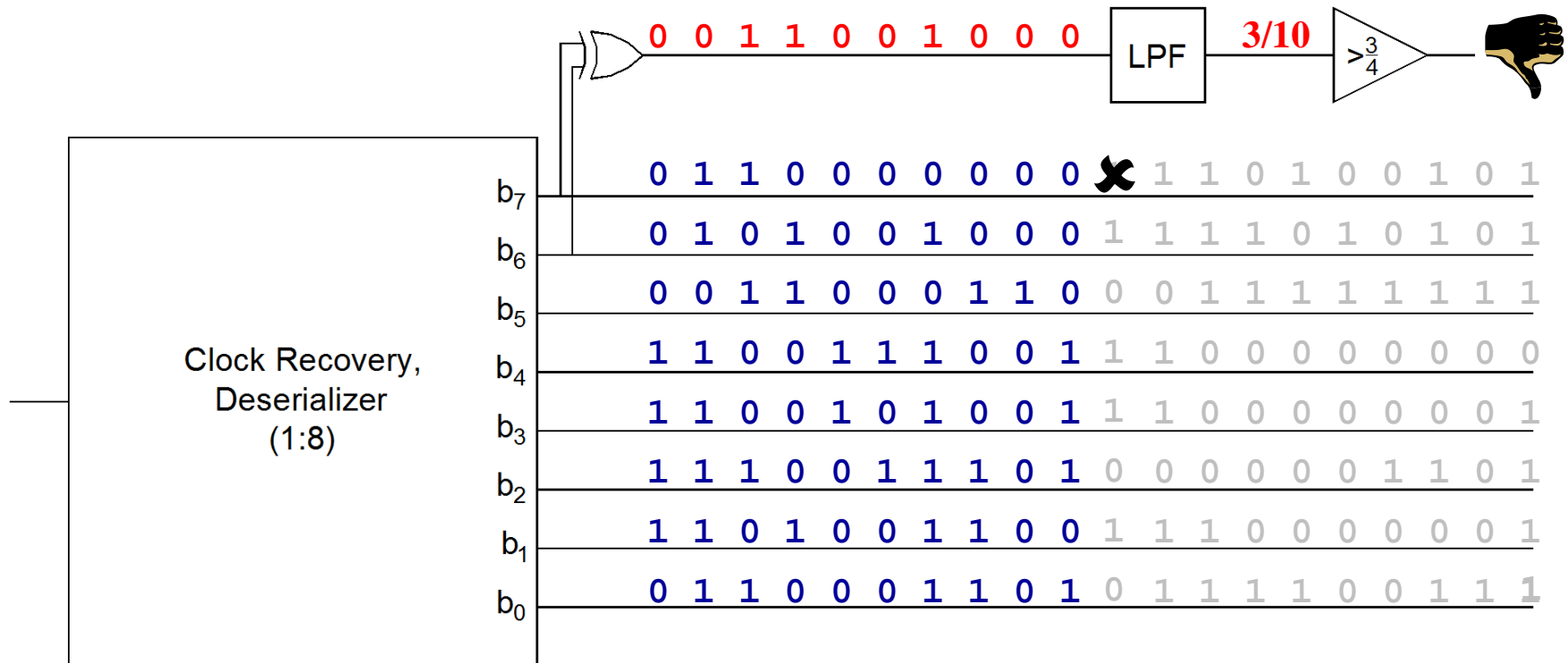
Trial Probability

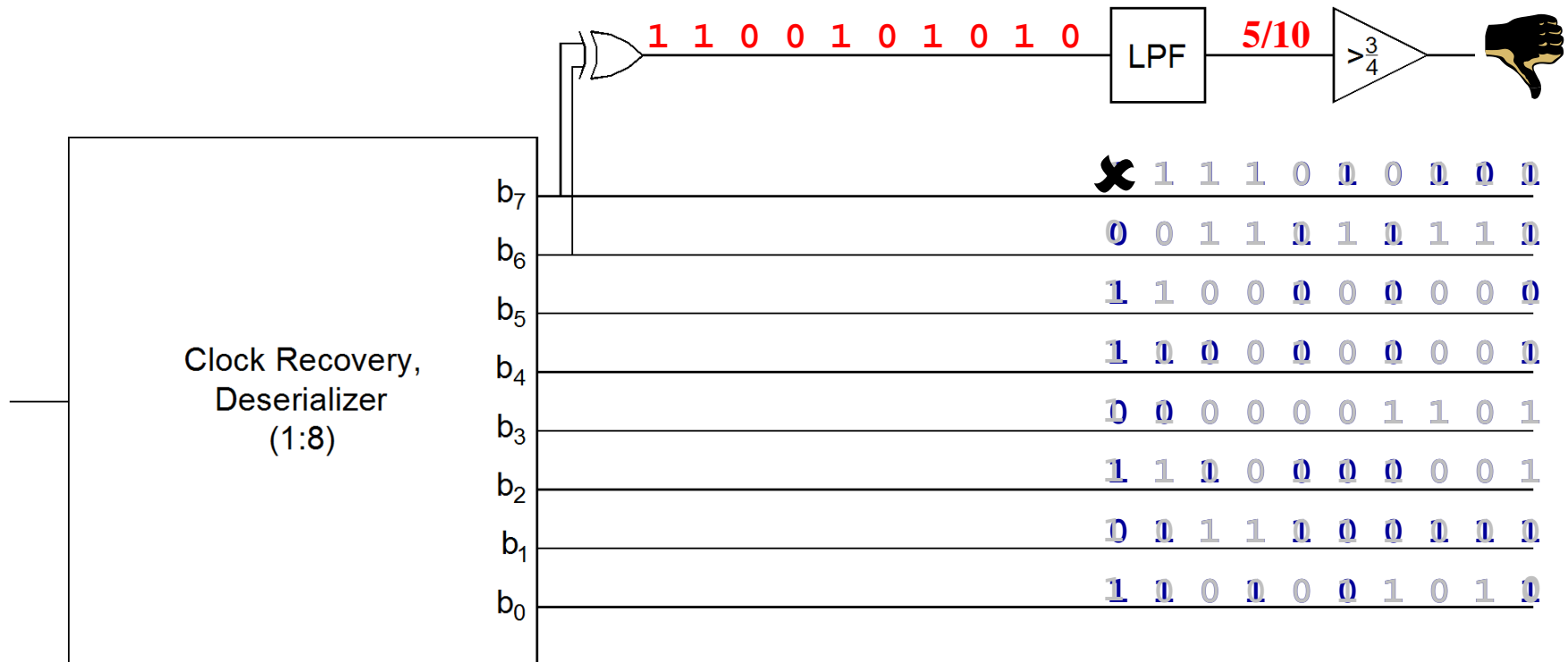Ensemble Distribution

ADC Saturation
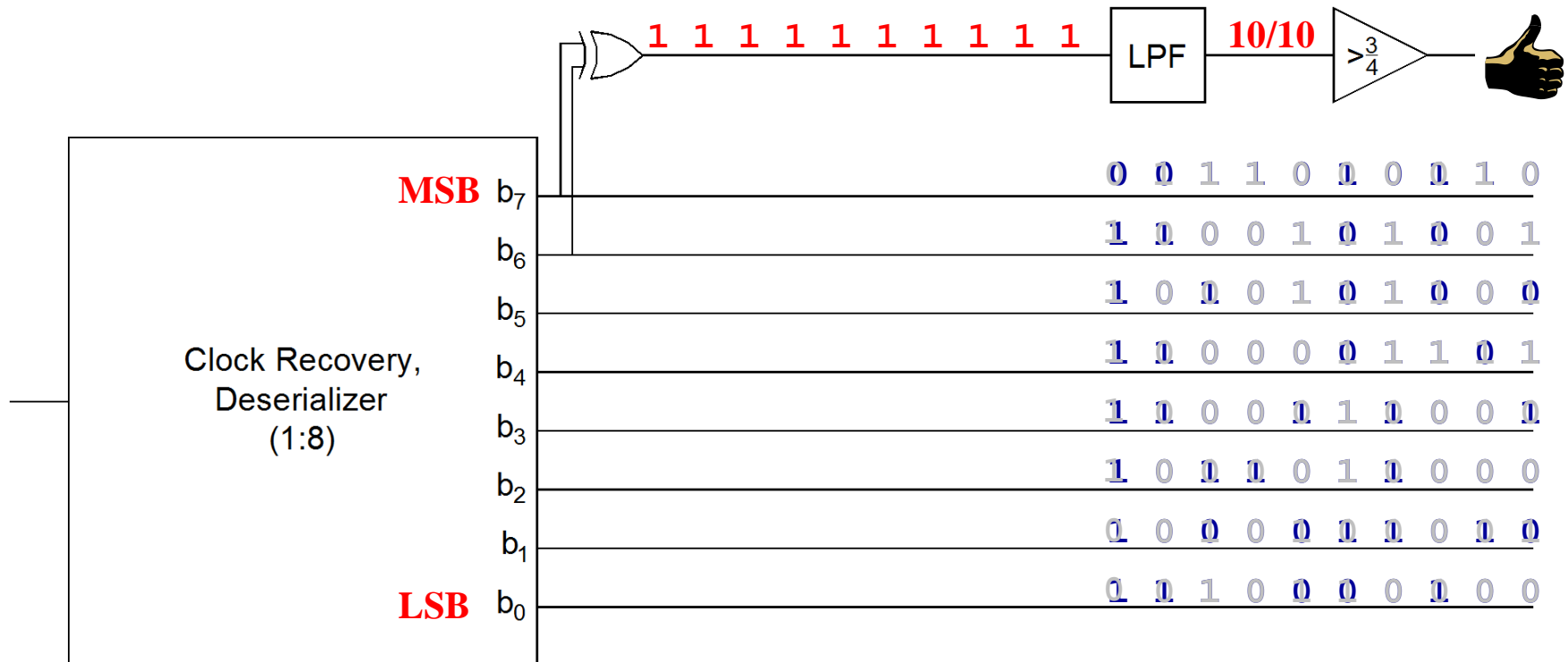
Non-Gaussian, Non-White Effects

Word Alignment – Where is the Most Significant Bit (MSB)?

# Word Alignment – Where is the Most Significant Bit (MSB)?

# Word Alignment – Where is the Most Significant Bit (MSB)?

# Bit Verification w/ Quadrature Sinusoids

- Noisy background largely removed by eliminating front-end gain.
  - some residual noise accounts for the dithering.

- Slightly mismatched gain as well as the expected quadrature phase is evident in the received waveform.

- Bit transmission errors would manifest as random outliers in the waveform, not nearby sample codes.
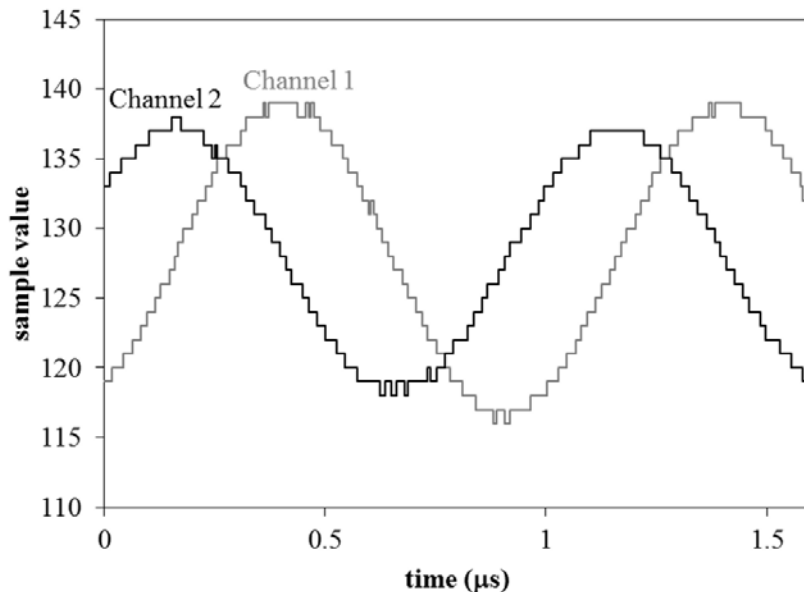
# Word Alignment Tests with Noisy Input
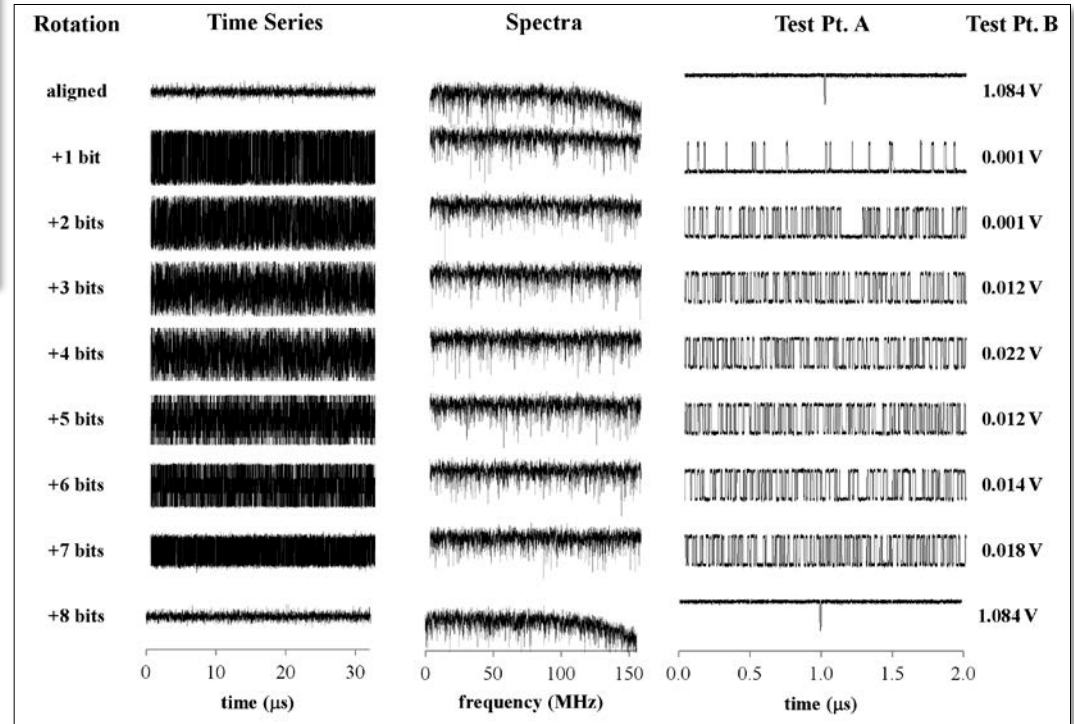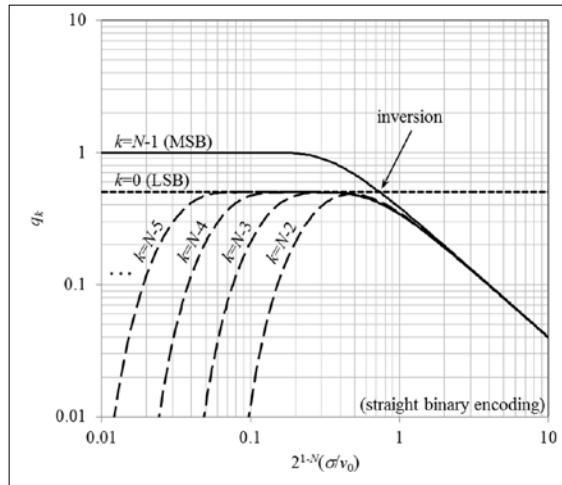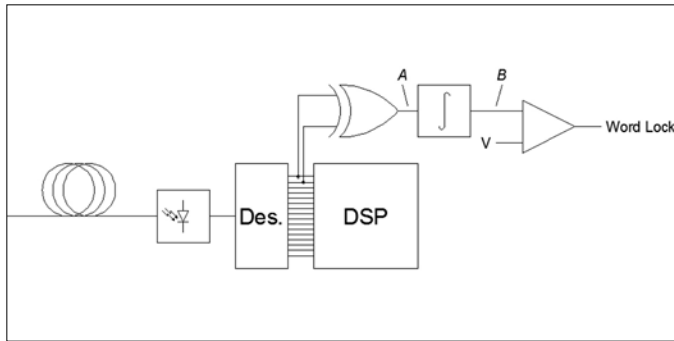
# Low Amplitude Failure (Clock Recovery)
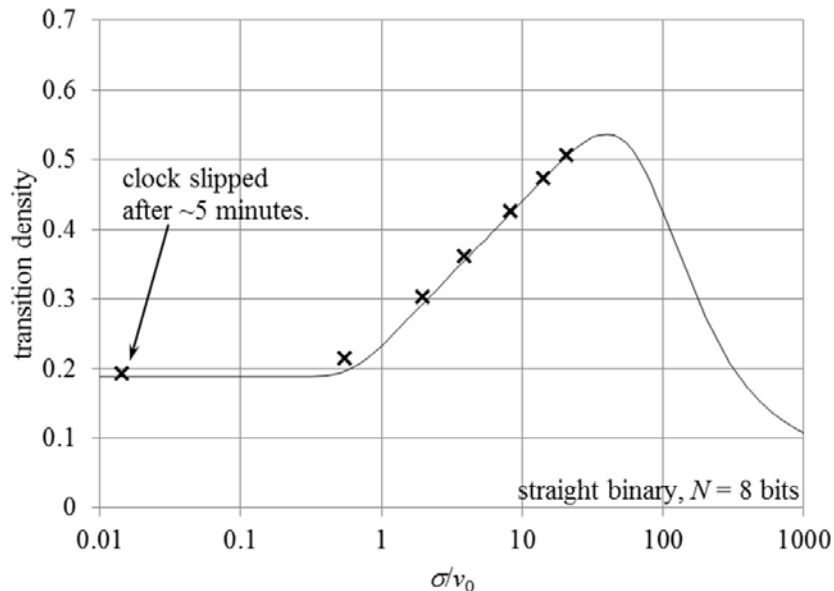
- Transition density reaches a minimum when rms amplitude drops below 1 sampler threshold.
  - zero crossings only
  - min. transition density = $1.5/N$

- Tested under this condition, the clock recovery loop failed after 5 minutes
  - approximately $1:10^{10}$ bits

- Bit slip detected immediately, realigned within milliseconds.

# High Amp. Failure (Word Alignment)
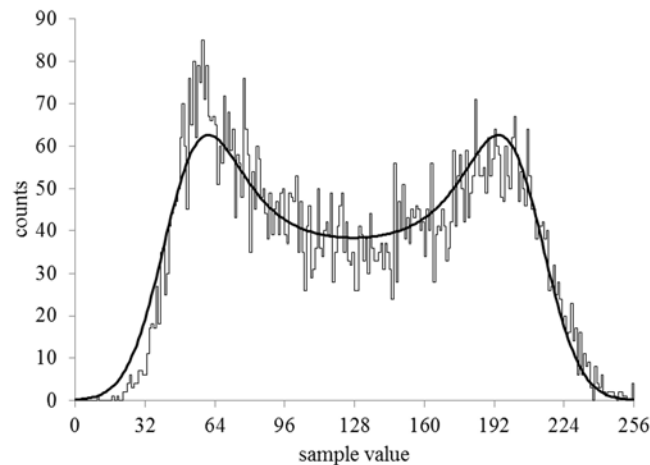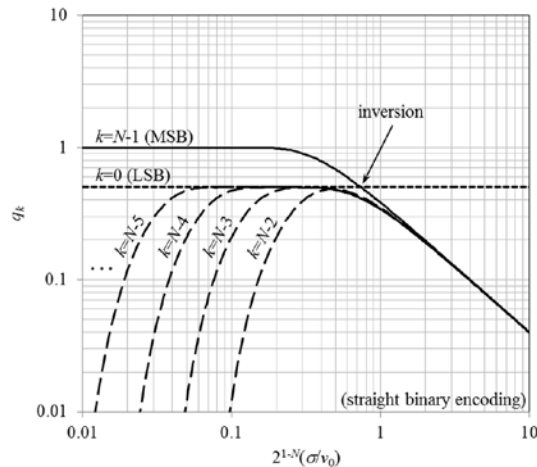
- Injected a large CW tone to invert histogram.
  - required a CW tone 14 times more powerful than the integrated noise.

- Causes the word boundary indicator to give a false indication that the MSB is not at the top pin of the deserializer, when in fact it still is.

- This effect is predictable if the rms is monitored, and could be confidently ignored.

40 Channel PAF Front-End (1.2-1.7 GHz)
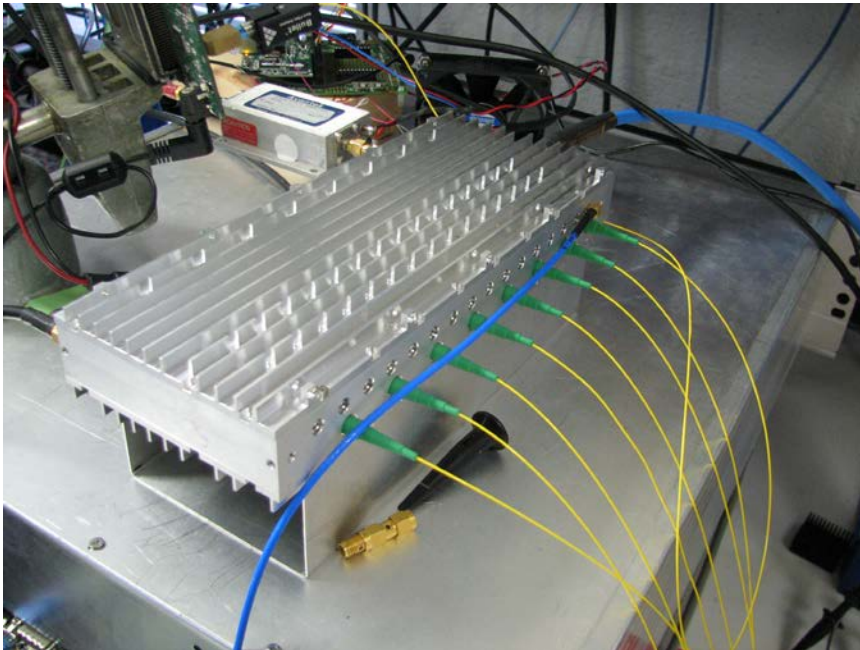
- Full RF-to-baseband-to-digital front-end with fiber outputs.
- 5 "blades" with 8 channels each (first blade shown at left)
- 100 Gbps total output.
- Complete 5-blade assembly measures roughly 4"x7"x9".
- Supporting Cryogenic Phased-Array-Feed instrument development program.

Multi-Channel Optical FPGA Interface
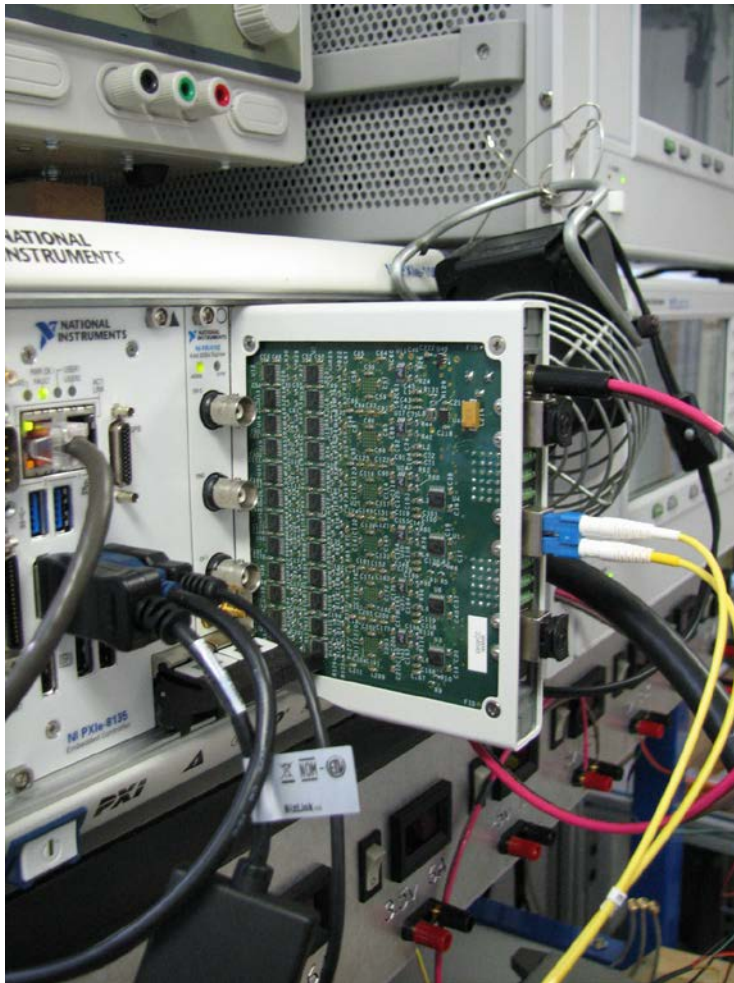

- Unit shown at left performs all link-management functions external to the FPGA
  - designed to emulate the ADC card which was formerly in the back-end attached to the FPGA.

- A much simpler version is being developed which performs only the optoelectronic conversion
  - data fed in to FPGA serially
  - link management performed by firmware

# Digital Output Spectrum (Unprocessed)
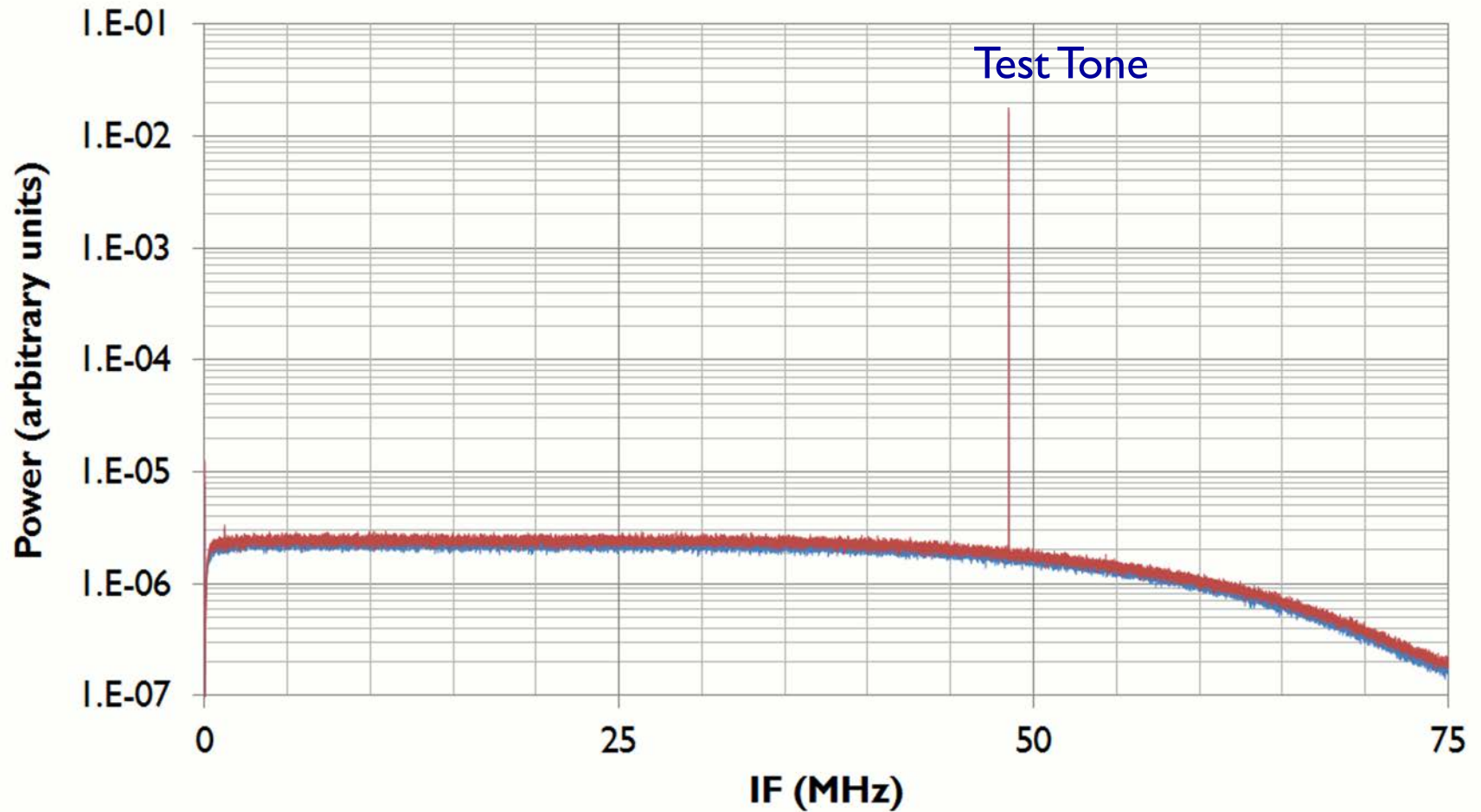
Serial-Output ADC Under Development

- Integration avoids power consumption in LVDS data transfer between ICs.

- Reduced footprint.

- Dynamically-variable sample-resolution.
    - Implementation should maintain power efficiency by utilizing only those comparators which are needed for the selected resolution.

- Serial rate = 40 Gbps

- Sample rate up to 20 GS/s

- Analog input BW up to 15 GHz
   - to support direct sampling of lower three bands.
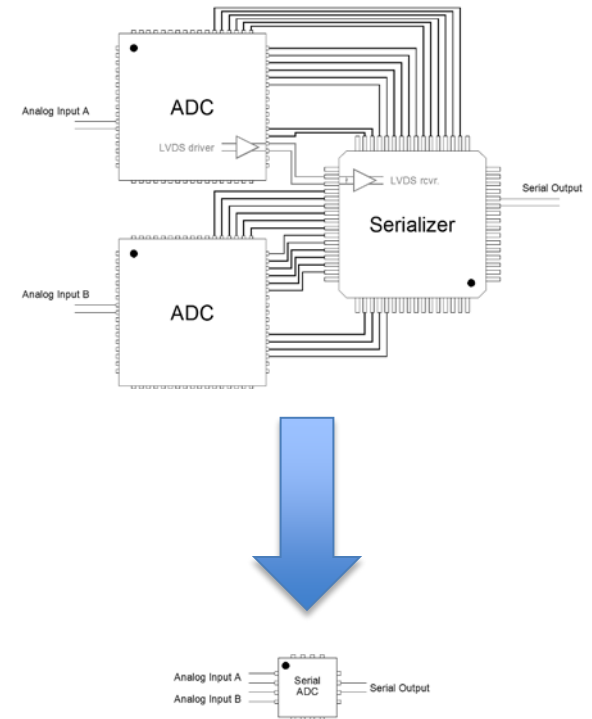
...and a De-Serializer...
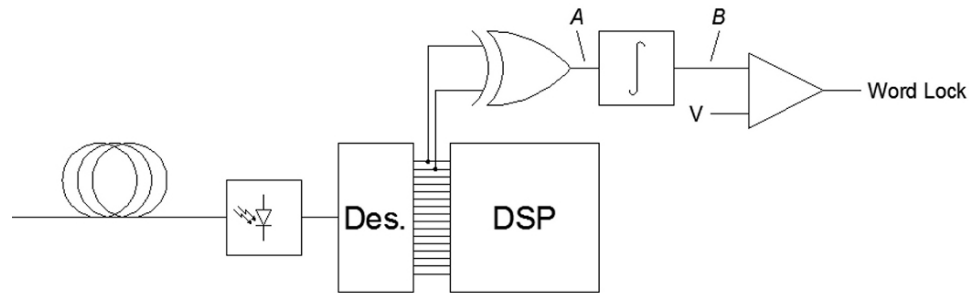
- 40 Gbps Clock Recovery
- Logic gates for alignment of the MSB in the unformatted bit-stream.
- Additional MSB-detection circuits for determination of resolution.

- *see M. Morgan, J. Fisher, and J. Castro, "Unformatted Digital Fiber-Optic Data Transmission for Radio Astronomy Front Ends," Publications of the Astronomical Society of the Pacific, vol. 125, no. 928, pp. 695-704, June 2013.*

...or De-Serialization Firmware.
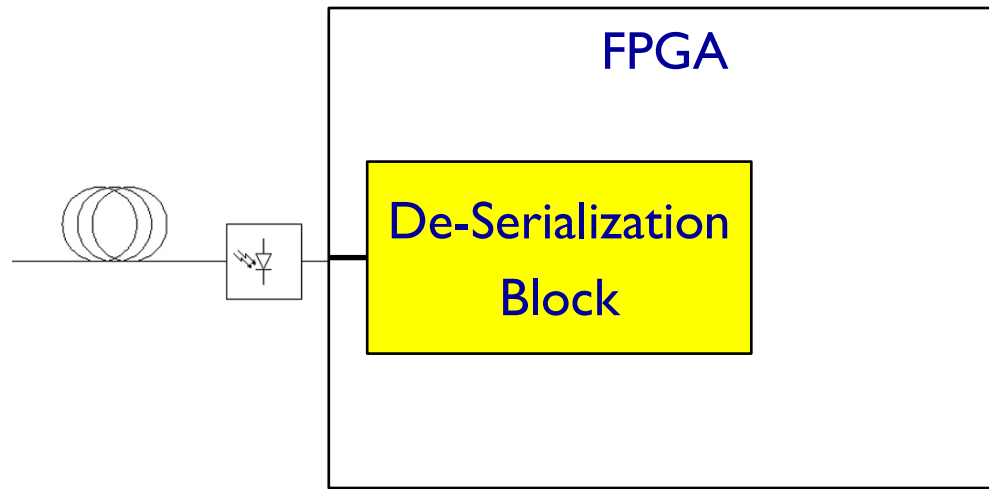
- If the FPGA has sufficiently fast serial inputs (40 Gbps), then all of the statistical de-serialization functionality could be implemented in firmware.