Abstract—This paper presents an implementation of a loaded transmission line as a voltage controlled phase shifter. This investigation concentrates on coplanar waveguide transmission lines loaded periodically with shottky diodes. A prototype is demonstrated exhibiting 55° of phase shift at 1.5GHz with $|S_{21}|=-3.5$ dB.

Keywords-component; Shottky Diode, Coplanar Wave Guide, Phase Shifter, Loaded Line.

I. INTRODUCTION

With the explosion in recent years of wireless communications, multi path systems, and phased array technology the need for robust, simple, cheap, phase shifters has likewise grown. One of the simplest and cheapest phase shifters to implement is the loaded line phase shifter.

II. LOADED LINE PHASE SHIFTER THEORY

The first step in understanding loaded line phase shifters is the basic lumped element transmission line model with series $L$ and shunt $C$ elements. From [1] the phase velocity along such a line is defined by (1).

$$v_p \frac{m}{s} = \frac{1}{\sqrt{L \frac{H}{m} + C \frac{F}{m}}}$$  \hspace{1cm} (1)

With a line of constant physical length, a phase shift can then be introduced by varying the phase velocity. A variable $L$ or $C$ is needed to vary $v_p$. A diode in reverse bias can function as such a variable capacitor. In a transmission line shunt loaded with diodes per Figure 1 the total capacitance, and hence the phase velocity, becomes a function of DC bias voltage per (2) where $l_{sec}$ is the physical length of a transmission line section in meters [2].

$$v_p \frac{m}{s} = \frac{1}{\sqrt{L \frac{H}{m} + C \frac{F}{m} + C_{var} \frac{F}{l_{sec} m}}}$$  \hspace{1cm} (2)

This lumped element transmission line model is limited to well below the Bragg frequency in (3), so named for the similarity to optical Bragg diffraction. In transmission lines the Bragg frequency corresponds to the frequency where $Z_0=0$ [3]. The reader will notice the similarity between the Bragg frequency expression and that for a standard LC low pass filter. The 3dB corner frequency of the LC filter occurs at exactly $\frac{1}{2}$ the theoretical Bragg frequency and is a good practical limit for the phase shifter operation of such a structure.

$$f_{Bragg} = \frac{1}{\pi \sqrt{L_d \frac{H}{C} \frac{F}{m} + C_{var} \frac{F}{l_{sec} m}}}$$  \hspace{1cm} (3)

III. DESIGN OF LOADED LINE PHASE SHIFTERS

Phase shifter design is well documented in the literature, [2],[4], and [5] but the design procedure outlined in [2] and [4] assumes an integrated circuit design with degrees of freedom in diode parameters. For this implementation a Hybrid Microwave Integrated Circuit (HMIC) similar to [5] is desired, but adapted to a higher frequency of operation. This requires altering the design equations given in [4] to make use of the degrees of freedom associated with the transmission line geometry.

The first design decision is, of course, which transmission line topology to use. Coplanar wave guide (CPW) was chosen for this investigation. CPW has some immediate advantages, first, both the ground and signal lines are in the same plane affording easy access for shunt mounting of elements without drilling. Second, CPW has a canonical closed form model from [6] that can be used to obtain design equations.
To maintain a balanced CPW line a balanced shunt loading topology was chosen with two shunt diodes per transmission line segment, one to each of the ground planes. This helps to ensure proper CPW operation. The drawback of this topology is it effectively halves the operating frequency by doubling the shunt capacitance. Other topologies are possible but require careful balancing of the ground planes.

In the HMIC case the variable capacitance parameters are set by the choice of diodes. There are several trade-offs in this selection. Obviously, from (3), a larger \( C_{\text{var}} \) will cause a reduction in the maximum operating frequency. Also the range of \( C_{\text{max}} \) to \( C_{\text{min}} \) will affect the variability of the phase velocity per (2) and hence the range of phase shift available. This is traded off with variations in the characteristic impedance of the line over \( C_{\text{var}} \) per (4) from [4], which is desired to be 50\( \Omega \) for impedance matching.

After experimenting with several diodes and matching schemes in simulation the Skyworks SMS3923 Schottky diode was chosen for its optimal matching characteristics. With a 2:1 specified \( C_{\text{max}} \) to \( C_{\text{min}} \) ratio this diode affords reasonable phase shift while allowing the transmission line to be well matched to 50 ohms without additional circuitry. From the Skyworks datasheet \( C_{\text{diode max}} \approx 1 \text{pF}, \) \( C_{\text{diode min}} \approx 0.5 \text{pF} \) giving \( C_{\text{max}} = 2 \text{pF} \) and \( C_{\text{min}} = 1 \text{pF} \) for the balanced topology chosen here.

After choosing an appropriate diode the remaining degrees of freedom are substrate choice and loading factor as defined by [4] in (5). For this implementation a 60mil single sided FR4 substrate was chosen to apply the ideal closed form CPW equations, to provide a mechanically stable base, and for its low cost. Loading factor trades off circuit size and diode losses versus CPW losses [2]. For FR4 CPW losses were negligible so the main trade off was size versus diode losses. A loading factor of 5 yields a circuit of a manageable physical size with respect to SMA connectors and the physical package size of the SMS3923-079 diodes and reasonable diode losses.

\[
x = \frac{C_{\text{max}} [F]}{l_{\text{sec}} [m]} \frac{C_d [F]}{m} \]

From these design choices the required CPW line parameters can be computed to give a 50\( \Omega \) matched line. From [4] the relation between loading factor and the characteristic impedance of the CPW line is given in (6). From \( C_{\text{max}} \) and \( x \) per (7) desired \( C_d \) is found. The open CPW closed form expressions given in [6] can then be used to compute the \( C[F/m] \) of the CPW line by (10) given \( Z_i \) from CPW equations (8) and (9). The length of each \( t \)-line section, \( l_{\text{sec}} \), is then given by (11).

\[
Z_i[\Omega] = 50 \sqrt{1 + x} \tag{6}
\]

\[
C_d = \frac{C_{\text{max}}}{x} \tag{7}
\]

\[
\varepsilon_r = \frac{\varepsilon_r + 1}{2} \tag{8}
\]

\[
KK = Z_i \frac{4 \sqrt{\varepsilon_r}}{120 \pi} \tag{9}
\]

\[
C \frac{F}{m} = \frac{4 \varepsilon_0 \varepsilon_r}{KK} \tag{10}
\]

\[
l_{\text{sec}} = \frac{C_d [F]}{C \frac{F}{m}} \tag{11}
\]

For \( x=5 \), SMS3923 diode, and 60mil FR4 the design parameters are: \( Z_i=122\Omega \), \( C_d=0.4 \text{pF} \), and \( l_{\text{sec}}=8.9\text{mm} \). These parameters are then input into Ansoft Designer, along with the SMS3923 diode model provided by Skyworks, to simulate this phase shifter. Designer computed dimensions for 122\( \Omega \) CPW as conductor width (W)=2.5mm, and gap width (G)=3mm. 50\( \Omega \) CPW for the biasing sections was computed to have W=2.5mm, G=0.25mm.

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![Figure 2. Ansoft Designer Schematic for Loaded Line.](image)

Generally the number of segments is chosen for a desired phase shift at an operating frequency. In this investigation
IV. SIMUALTION OF LOADED LINE PHASE SHIFTERS

Ansoft Designer was chosen for the circuit simulation of this design. All of the components can be well modeled in a circuit simulator, so a full wave simulation was deemed unnecessary. First, operation of the circuit was verified over the range of bias voltage to ensure the magnitude of the reflected and through S parameters stayed within reasonable bounds. As shown in Figure 3 |S11| is no less than 15 dB up to 1.6GHz and |S21| of no more than 6 dB.

![Figure 3. Simulated S Parameters Over Vbias](image)

Another application of this same structure is as a non-linear transmission line (NLTL). As an NLTL the non linear operation of the diode is used for wave shaping purposes to sharpen pulse edges. For phase shifting applications operation only in the linear region is desired. Generally this means that the input voltage magnitude must be small with respect to the forward voltage of the diode. In this case, as shown in Figure 4, this circuit is impeccably linear at 1 GHz and above even for very large input voltages. This is an advantage of operating near the LC filter corner frequency of the T-line model, all of the harmonic frequencies are severely attenuated. It should be noted at high input voltages that while the linearity of the phase shifter output is very good the significant loss due to diode rectification occurs.

![Figure 4. Time Domain NLTL Simulation Results](image)

A sweep showing phase shift versus bias voltage is given in Figure 5. In simulation we predict approximately 154° of phase shift at 1.5 GHz with a maximum |S21| at Vbias=0V of 5dB from Figure 3.

![Figure 5. Phase Shift versus Vbias at 1.5 GHz](image)

V. FABRICATION AND TESTING OF PHASE SHIFTERS

The final stage in this work was to fabricate and test a working prototype of this design. First, the CPW substrate geometry was drawn in AutoCAD. This geometry file was then exported to the milling workstation and used to control a precision milling machine to fabricate the CPW line with diode solder pads. The 1.6mm x 0.8mm diodes were then placed with tweezers on reflow solder paste beads. Next, the assembly was heated on a hot plate to solder the diodes in place. Finally, SMA connectors and DC blocking capacitors were soldered by hand onto the substrate. The final prototype is shown in Figure 6.
This prototype was then evaluated using a Vector Network Analyser (VNA) and a variable DC bias source. As shown in Figure 7 there is good agreement between measured and simulated S parameters at $V_{bias}=0V$. At $V_{bias}=20V$, per Figure 8, the measured and simulated results deviate quite significantly. In fact, the $V_{bias}=20V$ measurement results most closely matches the $V_{bias}=5V$ simulation. From the C vs V characteristic given in the SMS3923 datasheet we can interpret this as a significant reduction in $C_{max}/C_{min}$ ratio due to imperfections in the diode model and parasitics in the CPW diode mounting pad design. This reduction in capacitance ratio also explains our significantly reduced measured phase shift range as shown in Figure 9 versus simulated values of Figure 5.

The maximum $|S21|$ losses, at $V_{bias}=0V$, for the plots shown in Figure 9 were: $|S21(1.0GHz)|=-1.5dB$, $|S21(1.5GHz)|=-3.5dB$, $|S21(1.8GHz)|=-6.3dB$, and $|S21(2.0GHz)|=-14.3dB$. These figures yield $\phi/\text{dB}$ figures of merit of 18.7°/dB, 15.7°/dB, 12.8°/dB, and 4.4°/dB respectively. This prototype in the lower bands could well be applied to a narrow scan angle phased array, or a path synchronization problem. Alternatively to give a wider phase shift this prototype could be integrated with a 3-4 bit switched line for full 360° phase shift operation.

VI. CONCLUSIONS AND FUTURE WORK

In this work it has been shown that significant phase shift can be implemented cheaply and relatively easily using a loaded line phase shifter. It is also evident that device models and parasitics need to be carefully evaluated if designs are to show first pass agreement with simulations. Future work in this realm includes characterizing the diode used in-situ with the parasitics associated with the topology chosen to refine the simulation results. A diode with a higher specified capacitance ratio could be used at the cost of requiring a matching circuit. Anther option to extend the bandwidth of the circuit and reduce low pass filtering losses would be to offset the diodes to maintaining a pseudo...
balanced line at the cost of high input voltage linearity at lower frequencies.

Other lessons learned in this project include milling machine experience, proper reflow solder techniques, and experience interpreting time domain microwave simulations.

REFERENCES


