



April 2010
 Changed:
 R2 = 100 Ω
 C2 = 2 pF
 Normal voltage readings
 in red

NRAO DWG NO.
 B10803A012, Rev B. 4/14/2010
 CIT SOT PCB ASSEMBLY

Plated-thru via, .064" +/- .002" diameter after plating, 4 places
 Via X,Y locations relative to this corner

Material: Rogers Duroid 5870, .030" thick, double side copper, any thickness
 Gold plate for wire bonding
 Backside all copper (may be gold plated)
 Board size tolerance +/- .001

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 NAME: PCB for MIC SOT LNAs
 FILE: CITPCB3.dwg
 DATE: April 4, 2008
 BY: S. Weinreb