ALMA Backend Electronics Design Description

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Revision history

Rev	Approval Date	Part(s) affected	Reason/Remarks
A		All	First document release

Table of Contents

1. INTRODUCTION

1.1 Purpose

This document provides a design description for the Back End (BE) electronics.

1.2 Scope

The information contained in this document provides a design summary. There are no requirements in this document. Separate documents provide the requirements and specifications that must be met by the Back End Electronics design [AD2] and [AD3].

1.3 Reference documents

The documents in Table 2, below, are applicable documents. The revision level is the most recent at the time this document was submitted for approval.

Table 2. Applicable Documents

Reference	Document title	Document ID
[AD1]	ALMA System Design Description	ALMA 80.04.00.00-002-A-SPE
[AD2]	ALMA LO Reference and Timing Subsystem Design Specifications and Requirements	ALMA-50.00.00.00-076-A-SPE
[AD3]	ALMA IF Processing and Transmission Design Specifications and Requirements	ALMA-50.00.00.00-060-A-STD

1.4 Reference documents and drawings

Reference documents and drawings are listed in Table 3.

Table 3. Reference Documents and Drawings

Reference	Document title	Document ID
[R1]	List of acronyms and glossary for the ALMA project	(in preparation)
[R2]	ALMA Project Book	(obsolete)
[R3]	Operational Performance of the EVLA	EVLA Memo No. 43

[R5]	Digital Transmission System System Block Diagram	ALMA-80.04.01.00-004
[R6]	Digital Transmission System and Signaling Protocol, ALMA Memo no 420	
[R7]	Applicable entries in the ALMA Memo Series	

1.5 Acronyms

A limited set of basic acronyms used in this document is given below. A complete set of acronyms used in the ALMA project can be found in reference [R1].

AC	Alternating current
ACA	ALMA compact array (Japanese array)
ALMA	Atacama large millimeter array
AMCC	An IC vendor
ASIC	Application-specific IC
AOS	Array Operation Center
AOSTB	Array Operation Center Technical Building
BE	Back End
BER	Bit Error Rate
CAN	Serial bus by National Instruments used for M&C
CDR	Critical design review
CE	European standard equivalent to FCC Part B
CW	Continuous Wave
DAC	Digital to analog converter
DC	Direct current
DDS	Direct digital synthesizer
Demux	Demultiplexer
DG	Digitizer
DGCK	Digitizer clock
DGD	Sampler demux
DGS	Sampler
DTR	Deformatter
DTS	Digital transmission system
DTX	Formatter
DWDM	Dense WDM
EDFA	Erbium doped fiber amplifier (optical amplifier)

FPGA	Field programmable gate array (an IC)
FE	Front End
FO	Fiber optic
FOA	Fiber optic amplifier (EDFA)
FOD	FOA and DWDM demux assembles
FOP	Fiber optic patch panel
FOR	Fiber optic receiver
FOS	Fiber optic switch
FOX	Fiber optic transmitter
Gbps	Gigabits per second
Gsps	Giga samples per second
IC	Integrated circuit
ICD	Interface control document
IF	Intermediate frequency
IFDC	IF downconverter
IFMC	IF Monitor and Control
IFP	IF processor (Includes IFDC, IFBB, IFMC, and IFTP)
IFTP	IF Total Power Processor
I/Q mod	In-phase/quadrature modulator
LO	Local oscillator
LPF	Low pass filter
LSB	Least significant bit
LUT	
LVCMOS	Low voltage complementary metal oxide silica (an IC)
LVDS	Low voltage differential signal (used for accurate rise times)
MUX	Multiplexer
OC 192	SONET protocol for 10 Gbps link
PDR	Preliminary design review
PIN	P-region Intrinsic N-region (photodiode)
PS	Power Supply
RSC	Regional Science Center
SNR	Signal to Noise Ratio
SONET	Synchronous Optical Network (A communication standards organization)
SPST	Single pole single throw (a switch)
TUV	Europe equivalent to UL
UBC	Uniform Building Code
UL	Underwriters Lab (consumer protection code for appliance electrical wiring)
WDM	Wavelength Division Multiplexing
XMTR	Transmitter

2. DESCRIPTION

2.1. IF Processor (BE IFP) and Digital Transmission System (DTS)

2.1.1 Overview

The purpose of the IF Processing and signal transmission system is three fold:

a) Convert the IF received from the front end receiver electronics to wideband passband signals,
b) Digitize (quantize and sample) the passband signals, and
c) Transmit the digitized results to the correlator via a fiber optic data transmission system.

Simplified block diagrams appear in figures 1 and 2.

2.1.2 IF Processor

There are two IF (Intermediate Frequency) processors on each antenna, one for each polarization. There are up to four IF channels delivered from the front end: Upper sideband left polarization, lower sideband left polarization, upper sideband right polarization, and lower sideband right polarization. The IF signals from the active front end cartridge at each antenna pass through a multi-pole IF selector switch within the front-end package and then into the 1st-IF of the two IF downconverters. A downconverter provides gain, frequency translation, passband definition and total power data in the signal paths between the front end and the digitizers of the data transmission subsystem. Within a downconverter, frequency translation/tuning from each of the two input sidebands to the four output channels occurs by mixing with frequencies from a set of four second LO synthesizers (LO2-A, -B, -C, -D). The downconverter takes the wideband input signals of 4 - 12 GHz and produces four output signal channels, designated A, B, C, and D, with passbands of 2 - 4 GHz. The input and output noise-power distributions of the IF processors are nominally flat over their passbands. The module also performs total power measurements for both the wideband input signal channels and for the four output channels. Total power detectors provide astronomical data, such as continuum on-the-fly mapping. The 2nd-IF total power detectors also provide reference power levels to optimize input levels to the digitizers. The downconverters provide switching that allows any output channel to tune to either the high frequency (7.5 - 12 GHz) or low frequency (4 - 8.5 GHz) portion of either input channel. Bandpass filters for these frequency bands provide image suppression. Inputs in the 8 - 14 GHz range from four second LO synthesizers provide independent frequency tuning for the four 2nd-IF output channels.

2.1.3 Digitizer, sampler and demux– (DGD, DGS)

Each of the four baseband channels from a downconverter is sampled at 4 Gsamples/second to form a 3-bit 8-quantization level digital representation of the analog signal. Input/adapter/amplifier, comparators, associated latches, IF channels delivered, and encoding for the digitizer and output buffers are included within a single ASIC circuit (the digitizer sampler or DGS). The encoding permits easy identification of the digitized signal sign. There is one demultiplexing chip (DGD) for each of the 3-bit sampler outputs.Each DGD chip divides each sampler output by 16 to provide 250 Mbps signals to the DTS

formatter board. Thus, the digitizer demutiplexer board delivers 16 times 3 bits or 48 LVDS signals at 250 Mbps per digitizer.The DGS is clocked at 4 GHz and uses a sinusoidal signal delivered by the phase-controlled digitizer clock module. Each DGD chip receives the 4 GHz and 250 MHz clocks generated by the digitizer clock module and distributed by the digitizer assembly service board. The delay between these two clocks is adjusted with a capacitor on the DGD board.

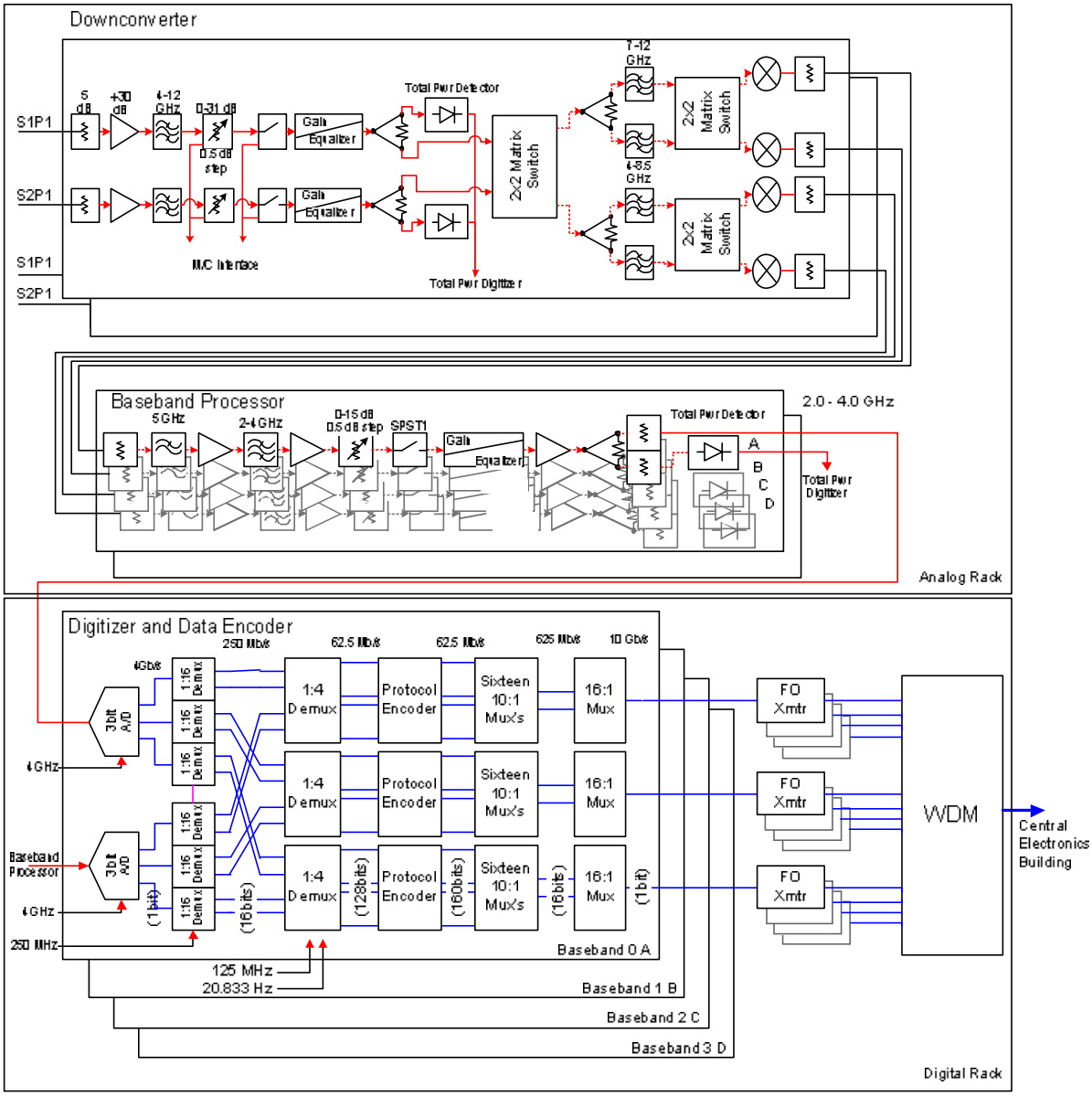

Figure 1. Back End – Simplified Block Diagram – Antenna Site

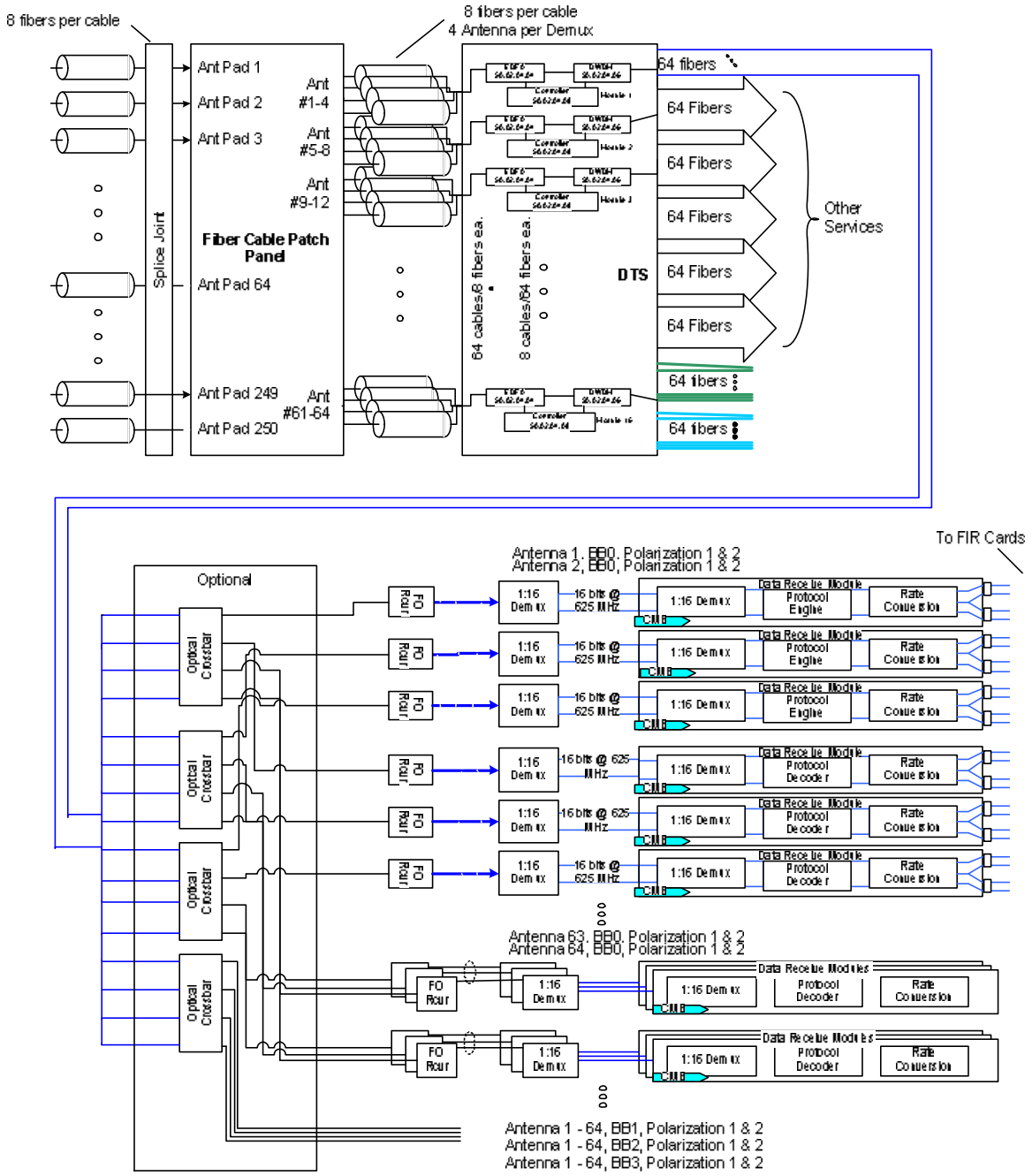

Figure 2. Back End – Simplified Block Diagram – AOS Technical Building

2.1.4 The digitizer clock (DGCK)

The digitizer clock module delivers a time-controlled 4 GHz signal to the digitizer assembly to implement the fractional part of the geometrical delay. Purely digital operations cannot provide more than 250 ps delay resolution, so a quasi-analog signal synthesis technique is used. The principle is to generate a 4 GHz sinewave, which is phase-steerable in 22.5 degree steps. This has the effect of shifting the time the sample is captured by 15.625 ps. The fractional part of the delay is written by the control software to the module every 48 ms. For long baselines, the delay needs to be refreshed more frequently, so an interpolation is performed locally.

Sixteen 1.4 degree steps are generated by a DDS chip at the convenient frequency of 7.8125 MHz (125/16). A second chip generates the same frequency with no phase shift. A pair of I/Q (in-phase/quadrature) modulators, configured as up and down frequency translators, export the synthesized phase shift to the frequency of 250.000 MHz. A phase-locked-loop multiplies this frequency by 16 to achieve 4 GHz. This last operation converts the 1.4 degree phase steps into 22.5 degrees as well.

The DGCK also delivers to the demultiplexer chip a 250 MHz signal whose timing coherently tracks the 4 GHz digitizer sampler timing. In addition, the DGCK delivers a fixed 250 MHz clock, generated from the fixed 125 MHz system clock to the Data Transmission System. The maximum timing swing between those two 250 MHz signal never exceeds 250 ps, compared with a period of 4 ns. This provides a wide timing zone where setup and hold timing conditions of the DTX input logic layers can be respected.

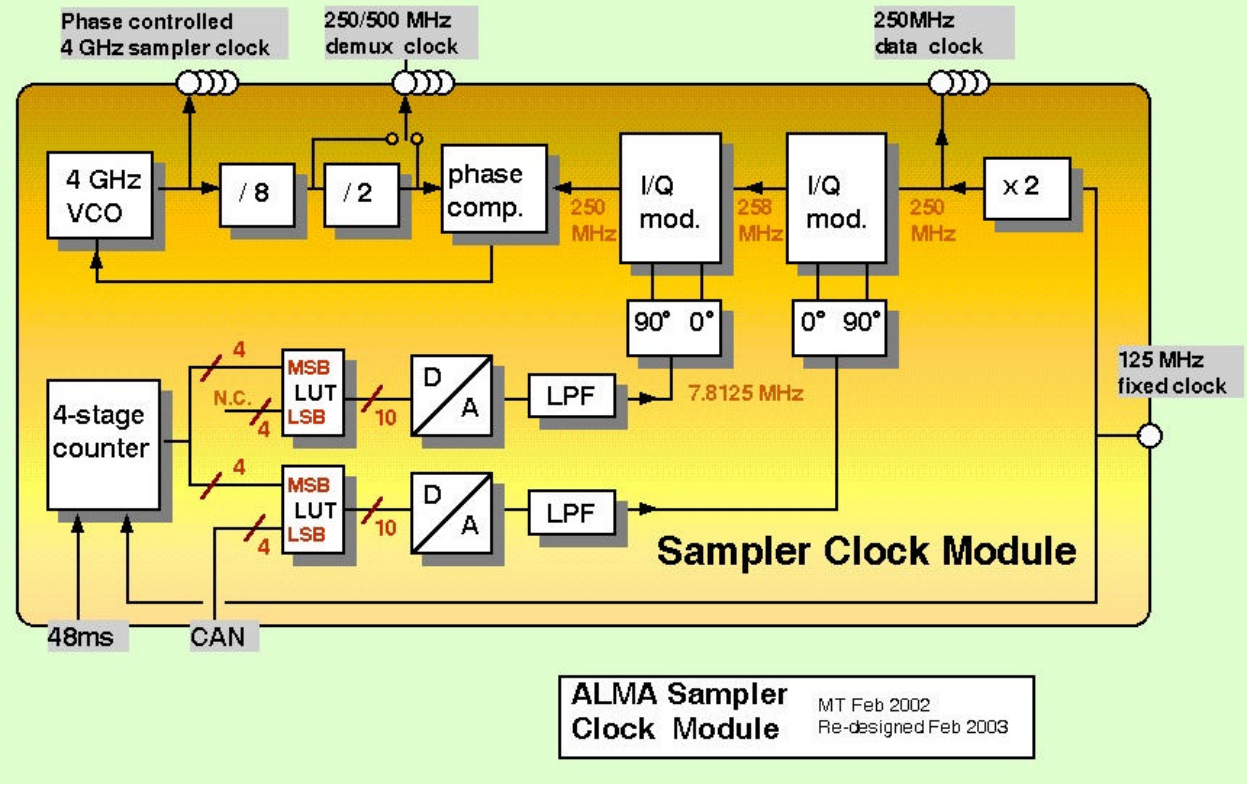

Figure 3. Sampler Clock block diagram

2.1.5 The digital fiber optic data transmission system

The Data Transmission System (DTS) is used to transmit the four digitized baseband (2 to 4 GHz) signals from each polarization to the Central Electronics Building. A sustained data rate of 10 Gbps per digital channel and 120 Gbits of formatted data per antenna is supported. The formatting overhead is 24 Gbps whereas the actual data rate is 96 Gbps per antenna (4 GspsX3bitX8 IF channels). Each digitized baseband pair uses a parallel interface of three 10 Gbps channels. Each set of three channels, twelve channels in total, is wavelength division multiplexed onto a single fiber for transmission to the correlator at the AOS Technical Building. The system configuration includes a CW laser, an Erbium Doped Fiber Amplifier (EDFA), passive optical multiplexers, up to 25 km of standard single mode fiber, and an optical receiver.

The transmitter/formatter hardware, located at the antenna, uses a Xilinx Virtex-2 series Field Programmable Gate Array (FPGA) to format the parallel 250 Mbps data from a pair of digitizers and configure it into serial data streams at 625 MHz. These data are then transferred to a 16:1 AMCC multiplexer intended for SONET OC192 communications. The device, which contains a phase-locked voltage controlled oscillator and a 16-bit shift register, produces a 10 Gbps serial data stream. An integrated optical transmitter module, containing a laser, a modulator driver amplifier and an electro absorptive (EA) optical modulator, is used to launch the 10 Gbps signal onto each of the twelve fibers at

twelve discrete wavelengths. The twelve fibers from the transmitters in each antenna are combined onto a single fiber using a passive 12:1 WDM fiber multiplexer.

The signaling protocol for the digital transmission is based upon a 160-bit frame structure using line coding employing scrambling techniques. The frame consists of a synchronization word, a sequence word, payload, and a checksum. Modulo-2 addition of the frame with a pseudo random pattern scrambles the data to provide adequate recovery timing information and a reduction of low frequency content. The 20% protocol overhead increases the overall transmission rate from 96 Gbps for data alone to 120 Gbps total rate from each antenna.

One digitizer assembly (2 samplers and 6 demux chips for two opposite polarizations), one-3 channel formatter, and the laser controller/transmitters are located in a single transmitter housing. There are four transmitter modules per antenna.

In the AOS Technical Building, the twelve optical signals from each antenna pad in use are routed to receiving equipment through a patch panel. The 12 signals are split apart using a passive WDM fiber de-multiplexer. Each optical carrier is fed to an SONET OC192-like optical receiver module, which contains a PIN photodiode, a trans-impedance amplifier and a limiting amplifier. The recovered 10 Gbits/s electrical data stream is fed to an AMCC 1:16 de-multiplexer IC. This device performs all clock and data recovery functions and de-multiplexes the data back into 16 serial data streams at 625 MHz. These data are then transferred using Low Voltage Differential Signaling (LVDS) to a Xilinx Virtex-2 Field Programmable Gate Array (FPGA). The Xilinx FPGA performs all synchronization, error checking, re-clocking and de-multiplexing functions. Data output to the Correlator is a 64 Bit wide LVCMOS word at 125 MHz per channel which preserves the original digitizer encoding.

2.2 LO Reference and Timing System

2.2.1 LO and time reference general description

The timing subsystem establishes all of the time synchronization in the array. The LO system provides the coherent frequencies to convert the received signals at each antenna from RF to IF to baseband and for tuning these signals for frequency and phase. A more detailed description of the LO and time reference subsystem can be found in [**AD21**] ALMA System Design Description.

2.2.2 H-maser

An hydrogen maser provides a frequency standard of 5 MHz to the Central Reference Generator. The H-maser is the array master oscillator. A crystal oscillator or rubidium oscillator may be substituted for non VLBI work.

2.2.3 Central reference generator/distributor

The central reference generator generates low frequency reference signals phase-locked to the 5 MHz input signal from the H-maser. The low frequency reference signals are: 48 ms (20.833 Hz), 25 MHz, 125 MHz, and 2 GHz. The central reference generator distributes the 5 MHz reference to the laser synthesizer microwave reference (DMR); the 25 MHz reference to the line length correctors and the CRD; the 125 MHz reference to the correlator; and the 2 GHz to the CRD.

The central reference distributor generates the master 48 ms timing reference and distributes it to the ARTM (RS-422) and to the Correlator (LVDS). The 25 MHz reference signal is modulated by the 48 ms timing signal, combined with the 2 GHz reference, modulated onto a DFB laser transmitter at 1532 nm, and distributed to all antennas as a composite signal on a single-mode optical fiber.

The low frequency, 20.833 Hz, is known as the 48 ms timing reference (1 / 20.833). The 20.833 Hz time reference is a logic waveform with a logic-1 state for a minimum of 1 microsecond and a maximum of 20% during each clock cycle. The rising edge of this waveform defines a timing event (TE).

2.2.4 LO reference receiver

The LO reference receiver is the master LO reference and timing distribution module at each antenna. It receives the LO reference composite 2 GHz signal on single-mode optical fiber and phase locks the low noise VCXOs to the incoming references for better phase noise and stability. The 25 MHz reference is used internally to offset the optical return for the line length correction system. The 125 MHz reference is distributed to the two Total Power Digitizer modules, to the four 2nd LO Synthesizers, to the DTS Sampler Clock module, and to the First LO Offset Generator (FLOOG). The 125 MHz harmonic generator output (8-14 GHz comb lines) is distributed to the four 2nd LO Synthesizers. The incoming 2 GHz reference is used (in conjunction with the 2 GHz comb line) to phase lock the 125 MHz VCXO used to generate the 8-14 GHz comb lines.

The LORR also recovers the 48 ms timing from the incoming 25 MHz reference and distributes it to: the ABM (RS-422), the four 2nd LO Synthesizers (LVDS), the DTS Sampler Clock module (LVDS), the four DTS Transmitter modules (LVDS), to the First LO Offset Generator (LVDS), and to the WVR.

2.2.5 Second LO Synthesizer

The conversion from IF to baseband requires LOs at 8-14 GHz. Four 2nd LO synthesizers are provided to allow independent tuning of each polarization-pair of 2 GHz baseband channels. The design covers the range in nominal 62.5 MHz steps, with the possibility of fine adjustable offsets of several MHz from the nominal frequencies using the fine tuning synthesizer as a reference for the tuning.

2.2.6 Fine tuning synthesizer

The fine tuning synthesizer is a direct digital synthesizer used to provide fine tuning, fringe tuning, phase switching and phase coherent frequency change capability to both the 1st LO Offset Generator and the 2nd LO synthesizer.

2.2.7 Photonic first LO reference

The ALMA First Local Oscillator is required to span 27-938 GHz in discrete bands. To do this, the output of a master laser is launched onto the LO fiber along with an offset frequency generated with a

laser synthesizer. The synthesizer is tuned by a variable frequency device called the microwave reference oscillator. There are 4 laser synthesizers, one for each subarray. Line length correctors on each fiber provide phase control of the reference frequencies.
The two wavelengths illuminate a photomixer which provides a difference frequency (beatnote) in the range 27-142 GHz to the 1st LO PLL. The 1st LO PLL is part of the LO Group and production responsibility belongs to the FE IPT. The photomixer that drives the PLL is also part of the LO Group but production belongs to the BE IPT. The warm multipliers which multiply the output of the photomixers likewise are part of the LO Group, but production belongs to the FE IPT.

At this writing, an intensity modulation scheme is being considered in view of relaxed phase stability requirements. Such a scheme would provide, for example, a 40 GHz LO to the antenna.

Central Local Oscillator Equipment

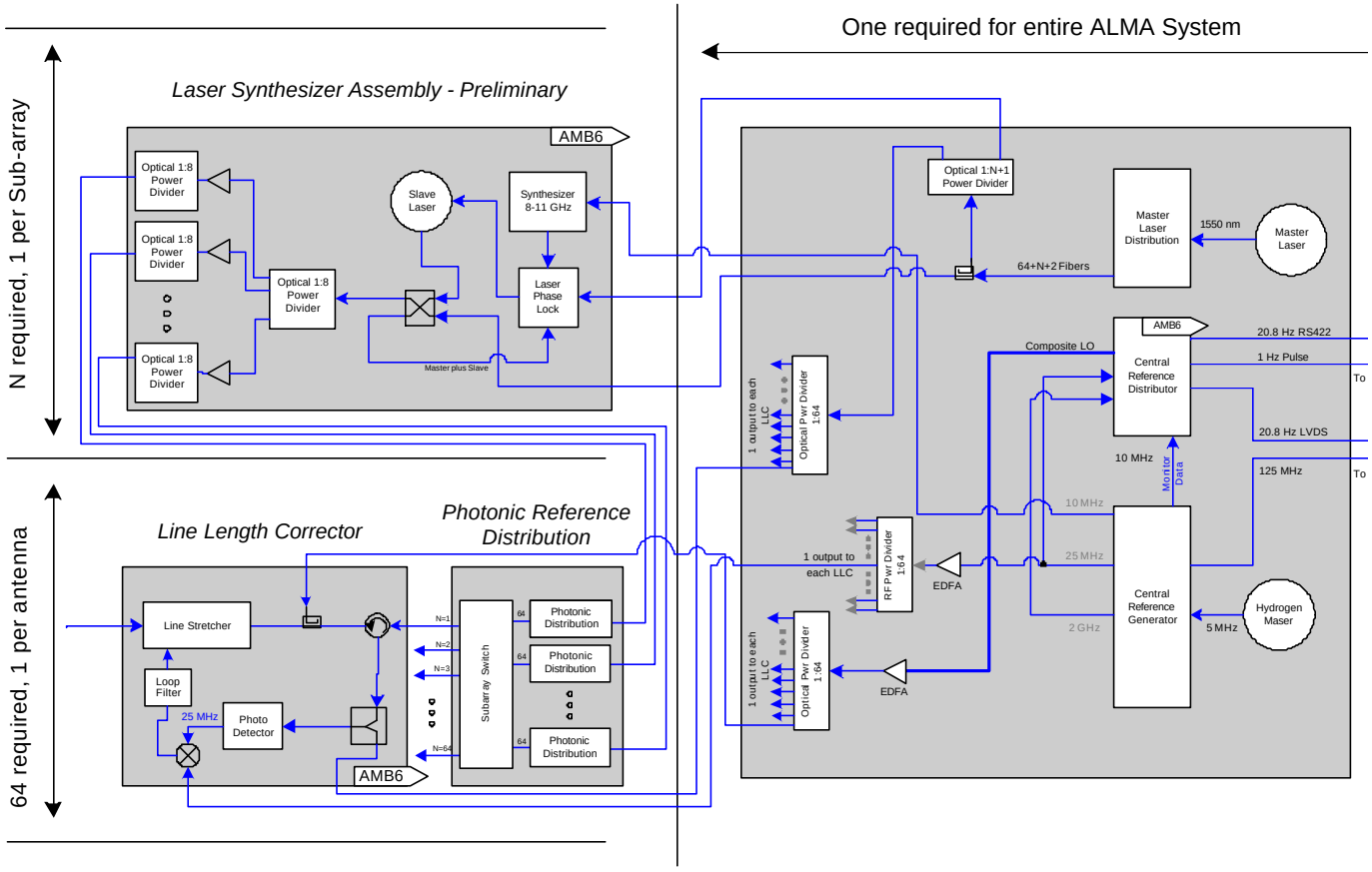

Figure 1. AOS TB Central LO equipment

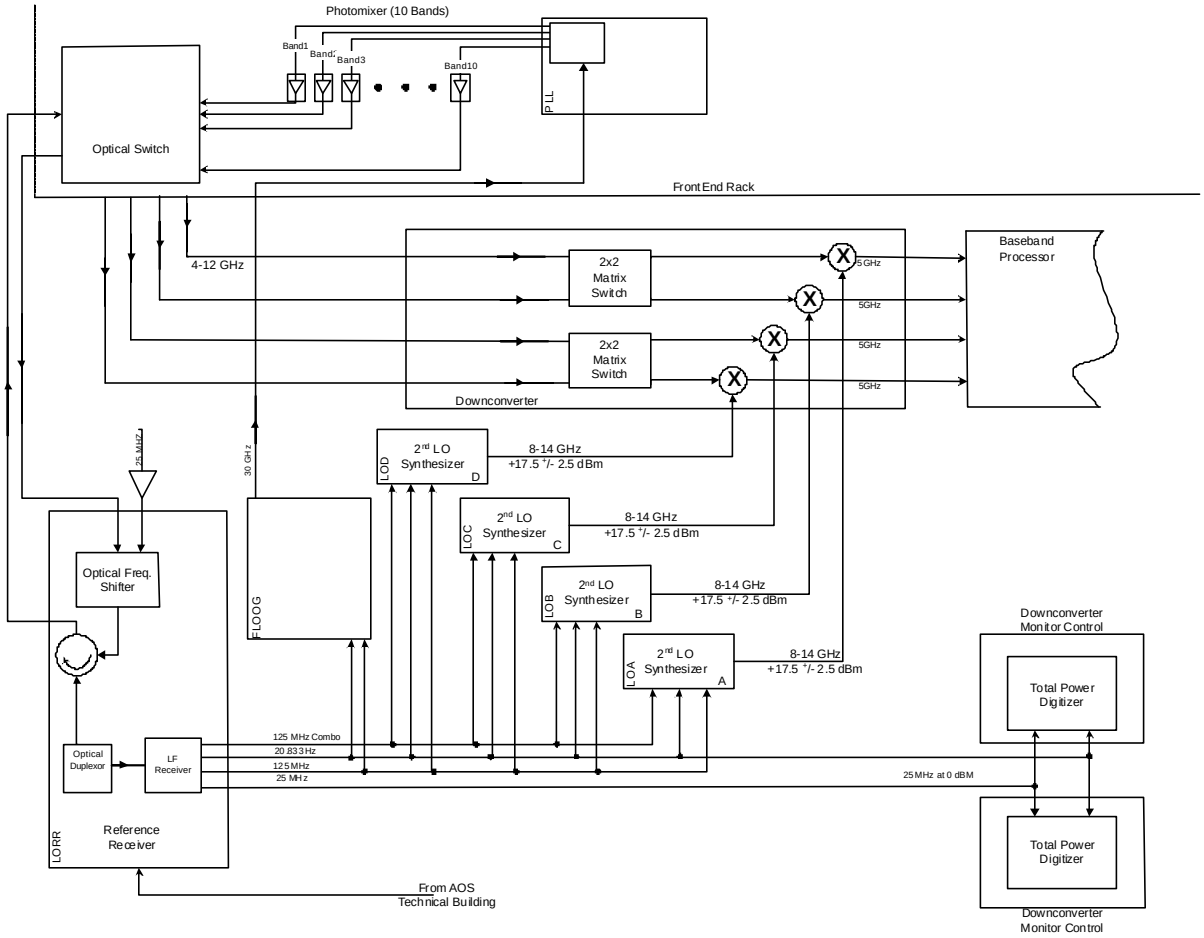

Figure 2. Simplified LO subsystem block diagram for antenna

2.3 Power Supplies and Hardware

The 230 VAC mains power is converted to 48 VDC by a commercial unit. Regulated DC voltages are converted from the 48 VDC by an in-house design power supply with M&C interface. Where other voltages are required or tighter regulation, power regulators and converters are provided within modules.

Module hardware is designed with RFI, thermal, connector stability, and ease of replacement in mind. The modules are mounted in bins using blind mate connectors where possible. The bins are

installed in standard equipment racks, shielded for RFI at the antenna and braced for Zone 4 seismic activity in the AOS TB.