



**Atacama  
Large  
Millimeter  
Array**

## **TUNABLE FILTER BANK CARD**


### **FUNCTIONAL DESCRIPTION**

Revision: B  
Status: Approved

CORL-60.01.07.00-001-B-SPE


2005-04-07

<b>Prepared By: Name(s) and Signature(s)</b>	<b>Organization</b>	<b>Date</b>
Giovanni COMORETTO Alain BAUDRY Benjamin QUERTIER Philippe CAIS Andre GUNST	IRAF, Osservatorio Astrofisico di Arcetri Univeristé de Bordeaux 1, Observatoire Univeristé de Bordeaux 1, Observatoire Univeristé de Bordeaux 1, Observatoire ASTRON, The Netherlands	
<b>Approved By IPT Name and Signature</b>	<b>Organization</b>	<b>Date</b>
A. BAUDRY	Observatoire de Bordeaux	2005-04-07
J. WEBBER	NRAO	
<b>Seen and Agreed By JAO Name and Signature</b>	<b>Organization</b>	<b>Date</b>
M. TARENGHI	JAO	

	<p align="center"><b>TUNABLE FILTER BANK CARD</b></p> <p align="center"><b>Functional Description</b></p>	<p>Doc: CORL-60.01.07.00-001-B-SPE  Date: 2005-04-07  Status: Approved  Page: 2 of 13</p>
---	---	---


### Change Record

Revision	Date	Affected Paragraphs(s)	Reason/Initiation/Remarks
A	2003-11-12	All	First issue
	2003-11-20		Changes (delay & various sections) from BAUDRY
	2003-11-25		Minor changes (various sections) from QUERTIER
	2003-11-27		COMORETTO adds various comments (mail of 27 Nov 03)
	2004-10-08		Reference documents added and minor corrections in different sections from BAUDRY.
	2004-10-12		Specifications revised to align document to current design COMORETTO
B	2005-04-07		Added 3 bit mode specs

	<p align="center"><b>TUNABLE FILTER BANK CARD</b></p> <p align="center"><b>Functional Description</b></p>	<p>Doc: CORL-60.01.07.00-001-B-SPE  Date: 2005-04-07  Status: Approved  Page: 3 of 13</p>
---	---	---

## TABLE OF CONTENTS

<b>1</b>	<b>PURPOSE OF THE DOCUMENT.....</b>	<b>4</b>
<b>2</b>	<b>RELATED DOCUMENTS AND DRAWINGS .....</b>	<b>4</b>
2.1	RELATED DOCUMENTS .....	4
2.2	RELATED INTERFACE DRAWINGS .....	4
2.3	ABBREVIATIONS AND ACRONYMS .....	4
<b>3</b>	<b>PHYSICAL INTERFACE .....</b>	<b>5</b>
3.1	CARD SIZE.....	5
3.2	CARD THICKNESS .....	5
3.3	CARD EJECTOR .....	5
<b>4</b>	<b>INPUT-OUTPUT INTERFACE .....</b>	<b>5</b>
<b>5</b>	<b>BOARD DESCRIPTION .....</b>	<b>6</b>
5.1	INTERFACE TO THE STATION BIN CONTROL COMPUTER .....	6
5.2	FINE DELAY .....	6
5.3	FIR FILTER ARRAY .....	6
<b>6</b>	<b>DETAILED DESCRIPTION OF EACH BLOCK.....</b>	<b>7</b>
6.1	CPLD2 INTERFACE.....	7
6.2	FINE DELAY .....	7
6.3	FIR FILTER.....	8
6.3.1	<i>Digital LO/Mixer.....</i>	<i>8</i>
6.3.2	<i>First Filter .....</i>	<i>9</i>
6.3.3	<i>Second Filter .....</i>	<i>10</i>
6.3.4	<i>Output Stage .....</i>	<i>11</i>
<b>7</b>	<b>OPERATING MODES.....</b>	<b>12</b>
7.1	TIME DIVISION (BYPASS) MODE.....	12
7.2	TIME DIVISION (BYPASS) 3-BIT MODE .....	12
7.3	FREQUENCY DIVISION MODE .....	12
7.4	OVERSAMPLED MODE .....	12
7.5	FOUR-BIT MODE .....	13
7.6	HALF-BANDWIDTH MODE .....	13

	<p align="center"><b>TUNABLE FILTER BANK CARD</b></p> <p align="center"><b>Functional Description</b></p>	<p>Doc: CORL-60.01.07.00-001-B-SPE  Date: 2005-04-07  Status: Approved  Page: 4 of 13</p>
---	---	---

## 1 PURPOSE OF THE DOCUMENT

This document describes the functionality of the Tunable Filter Bank (TFB) card, including all parameters that directly affect its performance, input and output signals, and programmable features.

Actual implementation and interfaces are described in other documents.

## 2 RELATED DOCUMENTS AND DRAWINGS

### 2.1 Related Documents

**RD01:** CORL-60.01.07.00-60.01.01.00-A-ICD

Internal ICD, From : Tunable Filter Bank Card To : Baseline Correlator

A. Baudry, J. Webber, C. Broadwell, P. Cais, G. Comoretto, R. Escoffier, A. Gunst, B. Quertier

**RD02:** CORL-60.00.00.00-020-A-MAN

Correlator Control Bus Manual

C. Broadwell

**RD03:** CORL-60.01.07.00-002-C-MAN

Programming Manual for Tunable Filter Bank

G. Comoretto

**RD04:** CORL-60.01.07.10-001-C-SOW

Statement of Work, Fabrication of Pre-Prototype Tunable Filter Bank Card

P. Cais (released to FEDD)

**RD05:** CORL-60.01.07.01-002-B-SOW

Statement of Work, Conception of the Prototype Tunable Filter Bank Card

P. Cais (released to FEE)

**RD06:** ALMA Memo 476 Enhancing the Baseline ALMA Correlator Performances with the Second Generation Correlator Digital Filter System

B. Quertier, G. Comoretto, A. Baudry, A. Gunst, A. Bos

**RD07:** CORL-60.01.07.01-010-A-SPE: Prototype Tunable Filter Bank card – Technical specification

G. Comoretto, A. Baudry, B. Quertier, P. Cais, A. Gunst

### 2.2 Related Interface Drawings


CORL-60.01.01.00-005-A-DWG      TFB Card ICD, Figures 1, 2 and 3

CORL-60.00.00.00-007-D-DWG      CPLD2 Chip Schematic Drawing

### 2.3 Abbreviations and Acronyms

A limited set of acronyms is given below.

ALMA	Atacama Large Millimeter Array
ASIC	Application Specific Integrated Circuit
AOS	Array Operations Site
DDS	Direct Digital Synthesizer
DTS	Data Transmission Subsystem

	<p style="text-align: center;"><b>TUNABLE FILTER BANK CARD</b></p> <p style="text-align: center;"><b>Functional Description</b></p>	<p>Doc: CORL-60.01.07.00-001-B-SPE  Date: 2005-04-07  Status: Approved  Page: 5 of 13</p>
--	---	---

ESO	European southern Observatory
FIR	Finite Impulsive Response (filter)
FPGA	Field Programmable Gate Array
IPT	Integrated Project Team
LO	Local Oscillator
NRAO	National Radio Astronomy Observatory
OSF	Operations Support Facility
PCB	Printed Circuit Board
TFB	Tunable Filter Bank

### 3 PHYSICAL INTERFACE

#### 3.1 Card Size

The filter card will be a 6U by 280 mm as seen in Fig2 of drawing CORL-60.01.01.00-005-A-ICD. A 6U is defined in VITA standards, see <http://www.vita.com/vso/draftstd/vita30-2001.d0.1a.pdf>

#### 3.2 Card Thickness

The filter card PCB thickness shall be 1.6 mm or 2.4 mm. If the PCB is 2.4 mm thick, the edges of the board that slides into the bin card guides shall be milled down to 1.6 mm. See Fig2 of drawing CORL-60.01.01.00-005-A-ICD for details, for measurement equivalents, and for tolerances.

#### 3.3 Card Ejector


The filter card will use card ejectors made by Scanbe (APW), or equivalent. If the filter card is 0.063 inches thick the correct Scanbe Part number is S-217. If the filter card is 0.093 inches thick the correct Scanbe Part number is S-217-100.

### 4 INPUT-OUTPUT INTERFACE

The board interfaces with the rest of the correlator subsystem via the station bin backplane. All power, data signals, controls, timing come from the backplane.

The board interface is composed of the following signals :

- Input data samples, as 32 3-bit consecutive samples, clocked at 125 MHz. Sample encoding is recovered from the decoders in the Fiber Optic card; it is Gray code as defined by the sampler ASIC designers.
- Output data samples : 32 2-bit samples, clocked at 125 MHz. Each sample represents the output of one independent FIR filter. Two 2-bit signals can be joined together to form a single 4-bit data stream.
- 125 MHz system clock
- 1ms signal, for synchronization with the array time. This signal is generated by the SCC. The signal has approximately 50% duty cycle, with rising edge on the 1ms time mark.

	<p align="center"><b>TUNABLE FILTER BANK CARD</b></p> <p align="center"><b>Functional Description</b></p>	<p>Doc: CORL-60.01.07.00-001-B-SPE  Date: 2005-04-07  Status: Approved  Page: 6 of 13</p>
---	---	---

- A RESET signal
- A standard microprocessor port, implemented using the standard CPLD1-CPLD2 interface, composed of :
  - o 8 bit data bus (bidirectional)
  - o 4 bit control bus
  - o a strobe pulse
- Two standard boundary scan 4-wire interfaces. One of the interfaces can be used to program the CPLD, the other is routed to a boundary scan loop crossing all the FPGAs in the board.
- A spare input
- A connection for the serial number-temperature sensor IC.
- Power supply pins including
  - o 3.3V supply (16 pins)
  - o 1.8V supply (44 pins)
  - o 5.0 V supply (1 pin)
  - o GND (46 pins)
  - o -48V (four -48V pins and five return pins, externally connected to GND, for FPGA internal 1.5 V supply).
- Voltage and current monitor pins for the internal 1.5V DC/DC converter. Current monitor pin produces a voltage with a scale factor of 50 mV/A.

An extra connector for debugging purpose is available on the front of the board. It provides 2 test points from each FPGA in the board. These lines can be used to monitor with an oscilloscope internal FPGA critical points, for debug and maintenance purpose.

Another connector on the front panel provides access to the temperature monitor diodes inside the larger FPGAs. An analog measuring circuit is required to probe these devices, e.g. a MAX 1617A or MAX1619 Digital Thermometer IC from Maxim. Diode characteristics are specified in Altera Stratix manual.

## 5 BOARD DESCRIPTION

The board implements the following functions :

### 5.1 Interface to the Station Bin Control Computer

It is composed by a standard CPLD (CPLD2 design), providing a common interface for all the boards in the correlator subsystem.


The interface allows individual FPGAs to be programmed/monitored, and to download FPGA personalities.

### 5.2 Fine Delay

This subsystem inserts a programmable delay in the input data stream, before it is fed to the FIR filters. The delay is in the range of 0 to 32K samples (plus a constant integer number of 32 sample blocks).

### 5.3 FIR Filter Array

A filter board is composed of an array of 32 identical filters. Each filter selects a subband of 62.5 MHz (max) and can be independently positioned within the 2 GHz input bandwidth. With degraded performances a bandwidth of 31.25 MHz can be

	<p style="text-align: center;"><b>TUNABLE FILTER BANK CARD</b></p> <p style="text-align: center;"><b>Functional Description</b></p>	<p>Doc: CORL-60.01.07.00-001-B-SPE  Date: 2005-04-07  Status: Approved  Page: 7 of 13</p>
---	---	---

selected for increased resolution using the correlator “oversample” option. The filter shape (and bandwidth) can be changed by loading appropriate filter taps. Band position is changed by programming a digital local oscillator.

## 6 DETAILED DESCRIPTION OF EACH BLOCK

### 6.1 CPLD2 Interface

The interface is seen as a block of 8 write and 8 read registers. The programming is described in more detail in document CORL-60.00.00.00-020-A-MAN Correlator Control Bus Manual.

Up to 16 individual FPGAs can be programmed, and each FPGA has an internal address space of up to 256 addresses. As the board contains 18 FPGAs (2 for delay and 16 FIR FPGAs) the FIR FPGAs are seen in couples, each one having up to 128 bytes of internal address space.

Addressing and programming details are given in the TFB Programming Manual.

### 6.2 Fine Delay

This subsystem inserts delays, with 250 ps steps in the range 0.0 ns to approx. 8  $\mu$ s. It operates together with the bulk delay subsystem (16 ns delay resolution at 125 MHz) which is part of the station board. It is implemented as a programmable barrel shift register, that shifts the input word of 32 samples by the required number of positions, plus a FIFO buffer for delays multiple of a 32 sample word. Each delay change becomes effective at the next system 1ms tick. (Sub-sample delay resolution is achieved in the digitizer by varying the sampler clock phase.)

Fine and bulk delay must be synchronously implemented. With the present configuration, synchronization does not account for the propagation time through the tunable filter board ; this is  $\sim$ 1024 samples, and is smeared by the filter response. The resulting phase glitch is about 500ns wide at most every minute. For this reason, an alternative strategy consists in keeping constant the bulk delay across an integration, and vary only the fine delay. A delay range of 8  $\mu$ s should allow up to 45 minutes of integration before the bulk delay should be readjusted.

The fine delay subsystem is composed of 3 identical segments, each one processing one data bit with the same delay. It acts also as a receiver buffer for the input data stream providing enough driving capabilities for signal distribution.

A Pseudorandom Data Generator is present at the input of the delay block and a corresponding data checker at its output. This is a standard feature present on all modules in the correlator data stream. Pseudorandom data can thus be inserted in place of the input signal, and/or checked for integrity.

Two test point signals can be selected from a number of internal signals and brought on the front connector.

#### **Input signal :**


3 bits, magnitude/sign Gray code

32 time multiplexed, 125 MHz clock, for a total of 4 GS/s

#### **Output signal :**

3 bits, magnitude/sign Gray code

32 time multiplexed, 125 MHz clock, for a total of 4 GS/s

	<b>TUNABLE FILTER BANK CARD</b>  <b>Functional Description</b>	Doc: CORL-60.01.07.00-001-B-SPE Date: 2005-04-07 Status: Approved Page: 8 of 13
---	--	--

### 6.3 FIR Filter

This system is described in detail in ALMA memo number 476 and references therein. The 32 individual filters are implemented in an array of 16 FPGAs. Each FPGA receives identical samples and produces two streams of non multiplexed 2-bit samples at 125 MHz. The filter can be completely bypassed, to operate the correlator in the original full bandwidth mode. In this case the output is one of the 32 input samples requantized to 2 bit.

**Input signal :**

3 bits, magnitude/sign Gray code

32 time multiplexed, 125 MHz clock, for a total of 4 GS/s

**Output signal :**

2 bits, real, signed binary code (as defined in the Correlator ASIC design)

4 bit modes available using two filters together

#### 6.3.1 Digital LO/Mixer

The mixer converts the input signal stream from 3 bit real to 2x6 bit complex. The input band is rotated cyclically in the frequency domain in order to have the centre of the desired band at frequency 0. Positive and negative frequencies represent different input frequencies. Each of the 32 time multiplexed streams is independently converted.

**Input signal :**

3 bit, magnitude/sign Gray code

32 time multiplexed, 125 MHz clock, for a total of 4 GS/s

**Output signal :**

6 bits, signed, with 1/2 level offset (values +/-0.5, +/-1.5 ... +/-31.5) complex real/imaginary, 32 time-multiplexed, 125 MS/s.

##### 6.3.1.1 Input stage


It receives the 32 parallel samples from the fine delay subsystem, and optionally check them with a pseudo random sequence checker. A 16 sample delay can be inserted for implementing a double Nyquist sampling mode.

##### 6.3.1.2 Local Oscillator (DDS)

Frequency resolution of the LO is 30.5 kHz (125 MHz/4096, 12-bit DDS accumulator), and frequency range is 0 to 2 GHz.

A separate register is used to load frequency. A load command transfers the frequency to the DDS register in synchronism with a specific 1ms pulse. The phase is cleared during load.

The DDS outputs a phase word of 9 bits (phase resolution 1/512 turn). Since the bulk delay is inserted after the frequency conversion, each time the delay is changed, the phase seen by the correlator also changes. A phase offset must then be added to the DDS phase to compensate for this. Phase offset is 16 bits. Phase change is also synchronized with a specific 1ms pulse.

	<p align="center"><b>TUNABLE FILTER BANK CARD</b></p> <p align="center"><b>Functional Description</b></p>	<p>Doc: CORL-60.01.07.00-001-B-SPE  Date: 2005-04-07  Status: Approved  Page: 9 of 13</p>
--	---	---

### **6.3.1.3 Mixer**

Each of the 32 input samples is converted independently, using a lookup memory. The memory contains 4 optimized quarter-sine tables. Each table corresponds to a quarter-sine multiplied by one of the 4 possible positive input values. Each table is 128 word x 5 bit wide, so that the 4 tables fit in a 512 x 5 bit read-only memory. Sign is treated externally and applied to the result to obtain a 6 bit signed value. Spurious and harmonic levels are below 50 dB of the carrier.

The LO phase is modified with the appropriate phase offset for the relative delay of the input sample,  $(F(LO) \cdot i \cdot 250\text{ps}, i=0..31)$ . Offset is automatically computed by the DDS when the frequency value is changed.

Both real and complex values are computed, using the dual-port feature of the FPGA internal memory.

## **6.3.2 First Filter**

This stage filters the converted input bandwidth to allow for decimation. The filter characteristics are listed below.

### **6.3.2.1 Filter Block**

Is composed of two identical FIR filters, for the real and imaginary parts of the signal.

Input: 32 x 6 bits

1/32 decimation

128 taps, using 64 multipliers implemented with lookup tables (LE in ALTERA terminology)

8 bit (7 + sign) coefficients, symmetrical, frozen

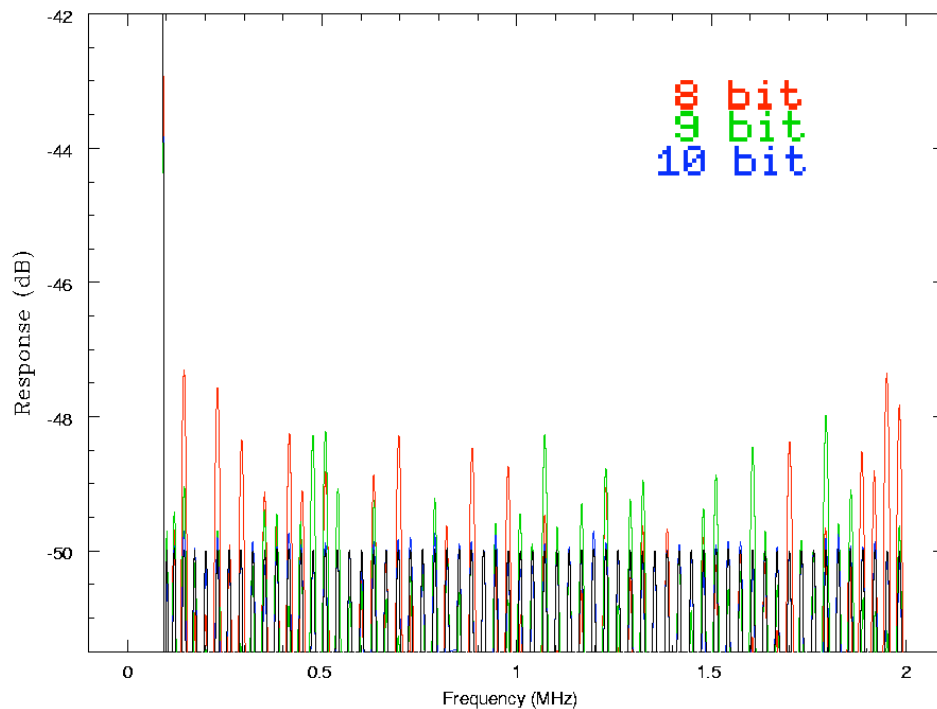
Addition of symmetric samples before multiplication

47 dB min stop band rejection, 50 dB average

Passband is +/- 31.25 MHz (1/32 of input bandwidth)

Guard bands are 62.5 MHz wide (from 31.25 to 93.75 MHz)

Roll-off in passband is < 1dB, compensated in second stage FIR



*Figure 1: Frequency response of the first filter. Actual response in red. Also shown are responses for 9 bit (green), 10 bit (blue) and infinite precision coefficients (black).*

#### **6.3.2.2 Full Scale Adder Tree and re-quantization**

The output from each tap multiplier is added with a full scale adder tree, giving a 19 bit output value. This value is re-quantized to a 8 bit signed output, with the following characteristics

- Output coding: \_ bit offset (values from -127.5 to +127.5).

- Quantization losses 0.05%

- Not adjustable for variable in-band power, can tolerate +/- 6 dB level variations

- Truncation error produces a DC offset at -80 dB with respect to the filtered noise

- Overflow correctly treated (mapped to maximum positive/negative values)

#### **6.3.3 Second Filter**

This stage determines the final bandwidth and shape. The filter shape can be changed by reloading tap coefficients, allowing for smaller output bandwidth (with poorer performances) or different trade-off of filter parameters. Parameters specified below refer to nominal tap coefficients.

##### **6.3.3.1 Filter Block**

Is composed of two identical FIR filters for the real and imaginary parts of the signal.

Input : 8 bit signed, real and imaginary samples, 2 x 125 MS/s

9 bit coefficients, identical for real and imaginary, loadable.

Nominal bandshape (can be changed by reloading taps):

	<p style="text-align: center;"><b>TUNABLE FILTER BANK CARD</b></p> <p style="text-align: center;"><b>Functional Description</b></p>	<p>Doc: CORL-60.01.07.00-001-B-SPE  Date: 2005-04-07  Status: Approved  Page: 11 of 13</p>
---	---	--

Bandwidth of +/- 29.3 MHz (15/32 of input band)  
Guard band of 3.9 MHz (2/32 of input band), symmetric with respect to band edges  
Stop band rejection > 45 dB  
In-band ripple < 0.2 dB p-p (first filter response included)  
Addition of symmetrical samples before multiplication  
Multiplication using DSP blocks (hardware 9 x 9 multipliers)  
Each band (real and imaginary) computes alternate output samples  
Full scale adder tree  
Output : 2 streams 62.5 MS/s (alternate real and imaginary, 125 MS/s total)

#### **6.3.3.2 Second Re-Quantization Stage**

Output of the adder tree is re-quantized to 9 bit  
9 bit signed output  
DC offset due to finite rounding (TBD)  
Quantization losses ~ 0.01%  
Not adjustable for variable in-band power, can tolerate +/- 6 dB level variations  
Overflow correctly treated (mapped to maximum positive./negative values)

### **6.3.4 Output Stage**

This section converts the complex filter output to a real value and performs 2-bit re-quantization for the correlator.

#### **6.3.4.1 Complex to Real Conversion**

Input : 2 streams (real & imaginary), 9 bits at 62.5 MS/s (interleaved)  
Output : 1 stream real, 9 bits at 125 MS/s

#### **6.3.4.2 Third Re-Quantization**

Input : 1 stream, real, 9 bits at 125 MS/s  
Output : 1 stream real, 2 bits, signed.

Re-quantization is performed multiplying the real stream by a programmable scale factor, and selecting two bits of the result.

There is the possibility of providing 4 bit quantization, using 2 filters for the same signal (thus on a maximum of 16 sub-channels): the filters compute exactly the same samples, and for one of the filters the next two bits of the rescaled result are selected.

The output data streams can be substituted with data produced by a 35 bit Pseudo Random Data Generator.

#### **6.3.4.3 Bypass mode**

The filter can be virtually excluded, to allow the correlator to operate in the original time multiplexed mode. In this mode one (selectable) of the 32 input samples is fed to the output. A fixed look-up table converts the input 3-bit Gray code to the 2 bit signed value required by the correlator. A 4 bit mode (actually only 3 bit are significant) is also available, using 2 filters for the same sample. In this mode, the two TFB are driven with the same signals, and the correlator processes only one polarization, with 64 spectral points per IF.

	<p align="center"><b>TUNABLE FILTER BANK CARD</b></p> <p align="center"><b>Functional Description</b></p>	<p>Doc: CORL-60.01.07.00-001-B-SPE  Date: 2005-04-07  Status: Approved  Page: 12 of 13</p>
---	---	--

#### **6.3.4.4 Total Power and Monitor**

Several monitor functions on the input and output signals are required. Measurements are performed using an accumulator that integrates the specified measure for an integration period. At the end of the period, results are stored in a register that can be accessed from the SCC.

Quantities that can be measured:

- Error rate in any of the input signals, using a Pseudo Random Data Checker
- Statistics on any of the input signals
- Statistics of any of the 8 input states on one of the 32 input samples
- Synchronization of the 3 bits for any of the 32 input samples
- Statistics of any of the 4 output states
- Digital total power on the second filter output, using a DSP multiplier as a square law detector.

The integrator has the following characteristics:

- Integration period : from 10 ms to 65s, in 1 ms steps.
- Programmable prescaler, to scale result in binary steps to the output register size.
- Output register size: 20 bits

## **7 OPERATING MODES**

Filter board can be operated in several modes, together with the station board. These modes allow to trade spectral resolution for sensitivity, or speed.

### **7.1 Time division (bypass) mode**

This mode is used mainly for fast integration and low spectral resolution observations. The filter bank is virtually excluded, and each filter simply re-quantizes one of the 32 time multiplexed inputs. The station board and the correlator operates in the baseline time division mode, with full 2 GHz bandwidth. Due to the low spectral resolution, this mode produces fewer correlation counts, and can be operated at the minimum integration time of 16 ms.

### **7.2 Time division (bypass) 3-bit mode**

This mode is analogous to the normal bypass mode, but each input sample is mapped to a 4-bit value (only 3 bits are significant, however). Both polarization channels are used to process the same signal, and the correlator is operated in 4-bit mode, with resolution reduced by a factor of 4. Only one polarization per IF can be processed, and the spectral resolution is 64 points/IF. The quantization loss is slightly worse with respect to the theoretical 3-bit value because the multiplication table is not optimal.

### **7.3 Frequency division mode**

Is the normal operation mode. Each filter is independently tuned to a different frequency within the 2 GHz input band. If less than 32 sub-channels are used, the station board can be used, together with the now available correlator planes, to provide extra correlation lags and increased spectral resolution.

### **7.4 Oversampled mode**

Filters are used in pair, with exactly the same setting, and one filter in each pair inserts a 16 sample delay at the input. All other filter parameters are set equal. In this way, the correlator analyzes a signal with the same bandwidth, but with doubled equivalent sampling rate, reducing quantization losses. At most 16 sub-channels can be used.

	<p style="text-align: center;"><b>TUNABLE FILTER BANK CARD</b></p> <p style="text-align: center;"><b>Functional Description</b></p>	<p>Doc: CORL-60.01.07.00-001-B-SPE  Date: 2005-04-07  Status: Approved  Page: 13 of 13</p>
--	---	--

### **7.5 Four-bit mode**

Filters are used in pair, with exactly the same setting. The output re-quantization circuit for one of the filters in each pair is modified in order to select the next two significant bits. Four correlator planes are required to compute a 4-bit x4-bit correlation product, with quantization losses largely reduced. At most 8 sub-channels can be used.

### **7.6 Half-bandwidth mode**

Reloading the filter taps, it is possible to reduce bandwidth to 31 MHz. The output data rate is also reduced to 62.5 MHz (two consecutive samples are always identical). Using the “oversample” mode in the correlator, it is possible to increase spectral resolution by a factor of 2, even if the number of spectral points remains the same. Modified filter has a much worse behaviour at the edges, and thus is not advisable (but also not useful) to stitch adjacent sub-channels.