Atacama
Large
Millimeter
Array

Software Development Plan for the Correlator Subsystem

COMP-70.40.00.00-002-C-PLA
Version: M
Status: Released
2006-12-18

Prepared By:		
Name(s) and Signature(s)	**Organization**	**Date**
Jim Pisano	NRAO	2006-12-18
Approved By:		
Name and Signature	**Organization**	**Date**
Brian Glendenning — Digitally signed by Brian Glendenning DN: cn=Brian Glendenning, c=US, o=ALMA/NRAO, ou=Computing IPT, email=bglenden@nrao.edu Reason: I am approving this document Date: 2007.04.18 13:16:26 -06'00'		
Released By:		
Name and Signature	**Organization**	**Date**

Change Record

Version	Date	Affected Section(s)	Change Request #	Reason/Initiation/Remarks
A		All		Incorporate external comments
B		Sec. 1, 2 & 4		Incorporate external comments
C		All		Released Version Incorporate comments from B. Glendenning & G. Raffi.
D	2002-11-19	4, 7		Updated schedule dates. Revised requirements matrix
E	2003-02-14	4		IDR changes
F	2003-05-16	4		PDR changes
H	2003-07-27	All		CDR1 changes
I	2004-05-18	All		CDR 2 preparations
J	2005-04-15	All		CDR 3 preparations
K	2005-06-15	All		Incorporate CDR 3 review comments
L	2006-04-17	Various		CDR 4 preparations Version ‘C’
M	2006-05-30	Various		Incorporate CDR 4 review comments
M	2006-12-18	All		CDR5 Updated

Table of Contents

1 Description 5
1.1 Purpose and Scope 5
1.2 Assumptions and Constraints 8
1.3 Deliverables 9
1.4 Schedule and Budget Summary 12
1.5 Document Scope 13
1.6 Document Evolution 13
1.7 Glossary 13
1.8 Applicable documents 14
1.9 References 14
2 Project Organization 14
2.1 Organization Interfaces 14
2.1.1 General Assumptions 14
2.2 Group Organization 15
2.3 Roles and Responsibilities 15
3 Managerial Process Plans 16
3.1 Start-up Plan 16
3.1.1 Estimates 16
3.1.2 Staffing 16
3.1.3 Staff Training 16
3.2 Work Plan 16
3.2.1 Work Breakdown Structure 16
3.2.2 Schedule Allocation 17
3.3 Project Tracking Plan 17
3.3.1 Requirements Management 17
3.3.2 Progress Control 17
3.3.3 Quality Control 17
3.3.4 Communication and Reporting 17
3.4 Risk Management Plan 17
3.5 Project Termination Plan 18
4 Technical Process Plans 18
4.1 Development Model 18
4.2 Release Issues 19
4.3 Methods and Tools 20
4.4 Infrastructure 20

4.5 Acceptance Plan 20
4.5.1 Acceptance Tests 20
5 Supporting Process Plan 20
5.1 Configuration Management 20
5.2 Validation 20
5.3 Documentation 20
5.4 Quality Assurance 20
5.5 Reviews 20
5.6 Problem Resolution 20
5.7 Process Improvement 21
6 Software Description 21
6.1 Software External interfaces 21
6.1.1 ACS Interfaces 21
6.1.2 Control Subsystem 21
6.1.3 Archive Subsystem 21
6.1.4 Observing Tool Subsystem 21
6.1.5 Data Capture (Offline Subsystem) 21
6.2 Software Design 21
6.3 Packages 22
6.4 Interfaces between Packages 23
6.5 Integration of Packages 23
7 Attachments 24
7.1 General Phase 2 Planning Model 24
7.2 Requirements Compliance Table 24
7.3 Computer Equipment Costs 31
7.4 Subsystem Concept 31

1 Description

1.1 Purpose and Scope

The purpose of the Correlator Subsystem is to provide a software interface to the configuration and status monitoring of the correlator hardware and the processing of raw lags into spectral channels. The subsystems which need to interface to the Correlator Subsystem are:

- **Control** – for configuration and monitoring of the correlator and as a conduit for other subsystems' need for correlator information.
- **Archive** – to store the raw science data blocks output from the correlator. Also CCC & CDP monitor data is stored in the archive. It is assumed that the archive subsystem will combine all the necessary data streams, monitor and data providing these combined data for other subsystems.
- **Telescope Calibration** – receives channel average data products
- **Quick Look Pipeline** – receives spectral and channel average data products
- **Executive** – receives integration events signaling the completion of an integration.
- **Offline** – DataCapture receives integration and sub-integration times and durations for subscans.

Figure 1 shows an architectural view of the correlator subsystem relative to other software subsystems with which it interfaces.

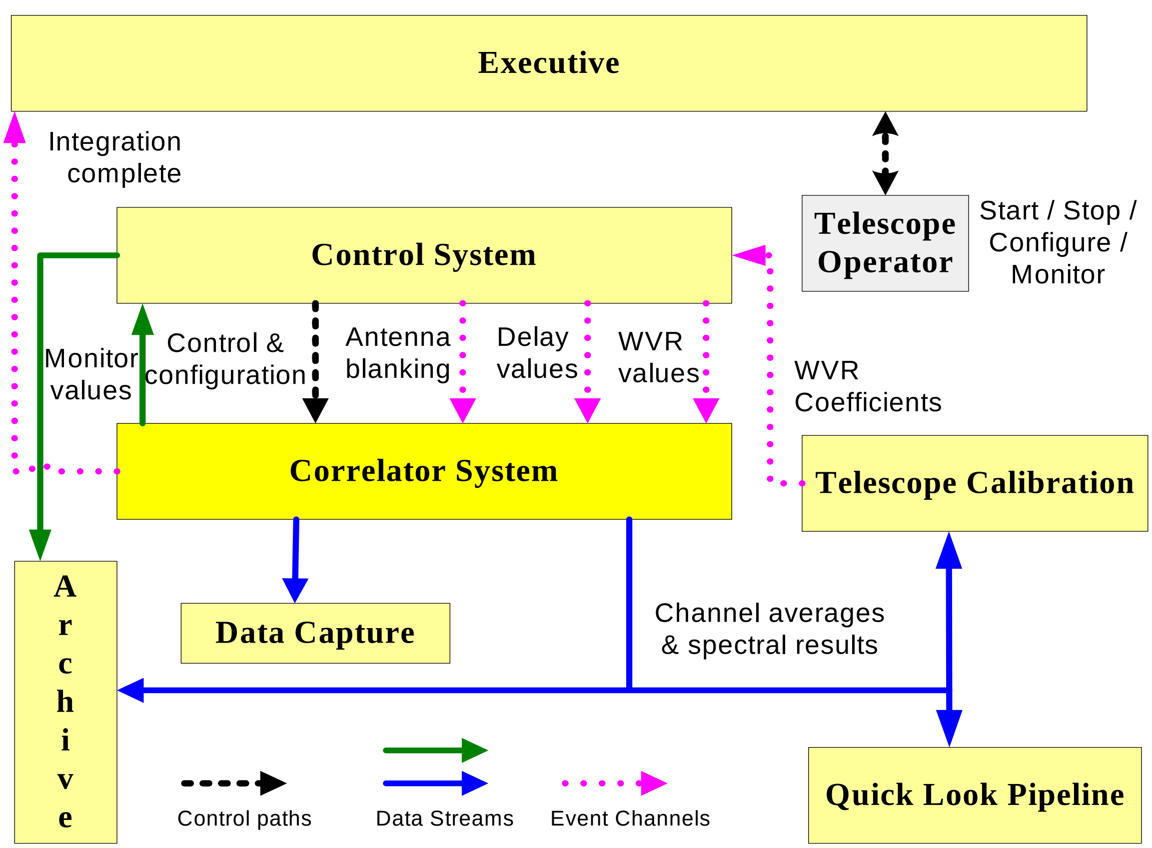

Figure 1 - Correlator Subsystem Architectural View

Figure 2 shows the physical layout of the Correlator Subsystem. The correlator computers are divided between the correlator control computer (CCC), which is a rack mounted PC, and the correlator data processing computer (CDP), which is based on a cluster of rack mounted PCs computers (see section 1.9, [ICD]). The CCC has the following network connections:

- CAN busses to the correlator quadrants for configuration and monitoring. There are three types of nodes in the correlator hardware; Long Term Accumulator (LTA), 'station controllers' (SCC), and quadrant control cards each of which have different control functions. It is currently planned to have 9 total CAN busses: four for LTAs, four for SCCs, and one for QCCs.

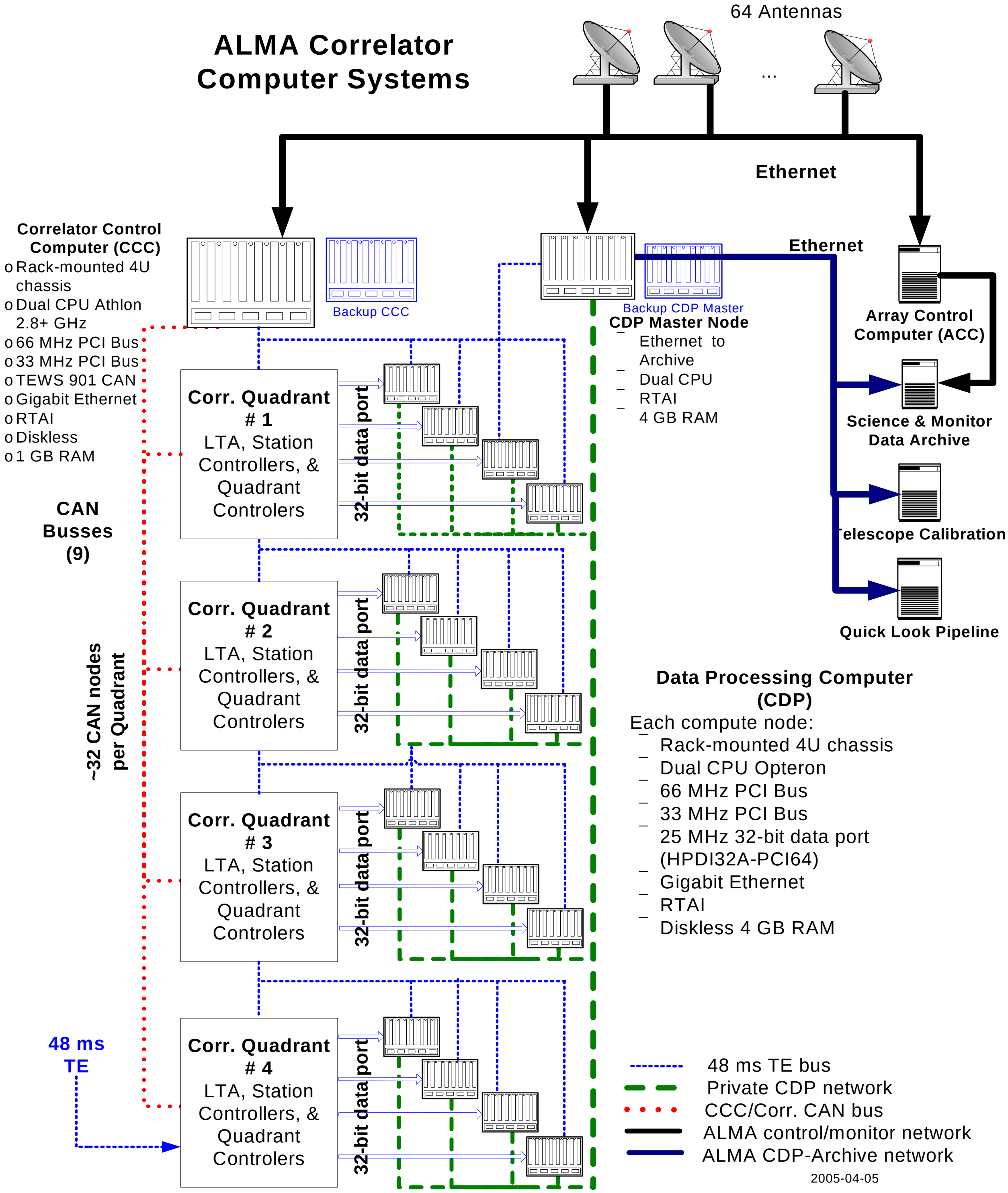

Figure 2 Correlator Computer Systems Layout

- High-speed Ethernet (e.g., Gigabit Ethernet) connection to the ACC at the OSF (Operations Support Facility) which commands the correlator. At this level, ACS will be used by client applications running on the ACC to interact with the CCC.
- High-speed Ethernet (e.g., Gigabit Ethernet) to the Antenna Bus Master (ABM) computers for real-time data channels.
- High-speed Ethernet (e.g., Gigabit Ethernet) connection to the CDP which acts as a conduit for data processing configuration information from the ACC. This part of the design provides a common point of control and configuration parameters for the CCC and CDP.

The CDP also appears in Figure 2. It is comprised of 16-node cluster plus a 'master' node. Its network interfaces include:

- 32-bit parallel data port connections to compute nodes. Each data port is capable of delivering 64MB/sec of raw lag data to each compute node. As currently designed all lags for a given baseline will come from one data port, i.e., baseline data will not span multiple data ports.
- High-speed Gigabit Ethernet connection among nodes. Spectral output after data processing of raw lags is transferred to the Archive computer via the master node.
- High-speed Ethernet (e.g., Gigabit Ethernet) connection to the CCC to receive data processing configuration information from the ACC.
- High-speed Ethernet (e.g., Gigabit Ethernet) connection to the ABM computers to receive real-time data during an sub-scan.
- High-speed Ethernet (e.g., Gigabit Ethernet) connection to the Archive computer to store raw science data blocks.

1.2 Assumptions and Constraints

The standards and procedures in [Plan] and [Practices] will be followed. Some of the main assumptions include:

- The Correlator systems software will be based on ALMA Common Software [ACS].
- RedHat Linux, with a patched kernel enabling the use of real-time Linux, RTAI [RTAI] will be utilized as a real-time kernel for the CCC and CDP computers.
- It is assumed that the Ethernet network between the output of the CDP to the Archive will support the maximum data rate (currently 60 MB/sec) not impinging on the CDP's ability to extract and process raw lags from the correlator. (Not for R4).
- The raw science data blocks published by the CDP will be routed directly into the BulkDataDistributor of the Archive using the ACS BulkData service.
- ACS will provide an output format of ACS::Time which supports resolutions of at least 100 nanoseconds.
- The Control system to supply geometric delays via a CORBA notification channel
- The Control system will supply antenna blanking events via a CORBA notification channel.

The correlator hardware delivery is a constraint. This risk is addressed in section 3.4.

The following external computer languages will be used: C++ using the GNU compilers, Python for developing unit tests, and Java for certain non-real-time components.

1.3 Deliverables

The deliverables will coincide with the availability of the various stages of correlator hardware. These are:

- **Release 0 2-antenna prototype correlator**

  Its purpose is to test out the correlator design and to support the two prototype antennas at the ATF. The software will support the correlator modes necessary to test out the correlator hardware in an operational environment and provide engineering support for the ATF. There are three bandwidth modes: 2 GHz, 250 MHz, and 31.25 MHz.

  Python scripts that act as ACS clients for configuration and data retrieval will be provided.

  Documentation to support the necessary tests will include interface documentation, user notes for Python scripts and engineering tests.

  No computer equipment will be delivered.

  Status: Done

- **Release 1.0 2-antenna prototype correlator**

  This release will be an enhanced version of software for support of the 2-antenna prototype correlator. It will be delivered to the AOC for SI (System Integration) testing of the signal chain – evaluation receivers to correlator.

  A limited correlator simulator will be provided that:

  - accepts a CorrelatorConfiguration data entity from the control system, validate it (from the correlator ICD [ICD]: ObservationControl::configureSubScan(), ConfigurationValidator::isValid(), ConfigurationValidator::getInvalidConfigurationItems())
  - accepts GeometricDelayModel events from the control system
  - publishes some monitor events
  - publishes PublishIntegration events
  - publishes ‘sample’ spectral data using a preliminary VOTable format

  Limited support for interfacing to the other subsystems in listed section 1.1 will be included.

  Documentation which covers the enhancements introduced in Release 1.0 will be provided.

  The following computer equipment will be delivered to the ATF:

  - VME crate with PowerPC CPU board, CAN controller. Note that the PowerPC CPU board will be replaced by a VMIC 7766 Intel CPU board.
  - 2 dual-CPU PCs with 2.0+ GHz Athlon processors, 66 MHz bus. Note that the CPU choice and speed may change, but will stay current of the latest available hardware.

- 1 PCI64-HPDI32A data port interface card
- 1 RS-485 PCI interface card for master node TE interface
- 100 Mbps hub

Status: Done

- **Release 2.0 2 antenna prototype correlator, 16-antenna single quadrant correlator, correlator hardware simulator**

Further enhancements for the 2 antenna prototype correlator for the ATF test interferometer. This software will support the observing mode *Single field interferometry* at the ATF and various engineering tests.

The first production correlator consists of one quadrant and supports up to 16 antennas in Chile. Correlator software will be based on the two antenna prototype but expanded to support many requirements in [SSR].

A simulator for the correlator hardware will be developed. This software will simulate control and monitoring via the CCC and generate simulated lag data for FFT processing in the CDP. Its purpose will provide support for integration testing when correlator hardware is not available. The simulator will incorporate ACS interfaces and use RTAI.

This release will also support prototyping work for the full CDP to assess the scaling and data loading issues related to the full four-quadrant correlator although this hardware will not be delivered to the ATF. This performance testing will be used to determine if the current design is adequate and if not, a back-up plan will be devised.

- 1 dual-CPU rack-mounted PC with 2.8+ GHz Athlon processors.
- 4 dual-CPU PCs with 2.8+ GHz Athlon processors, 66 MHz bus. Note that the CPU choice and speed may change, but will stay current of the latest available hardware.
- 4 PCI64-HPDI32A data port interface card
- 2 RS-485 PCI interface cards for master node TE interface
- 1 TPI901 CAN card + PMC-to-PCI carrier card
- 1 Gigabit router for lab tests

Status: Done

- **Release 3.0 Enhanced support for the 2-antenna correlator, prototyping support for the 16-antenna, one-quadrant correlator**

This release will provide enhanced support for the 2 antenna system and should coincide with the prototype correlator delivery to the ATF. This enhancement will address robustness and more features which satisfy requirements in [Requirements]. Prototyping work on the 16-antenna, 1quadrant correlator will begin.

Python scripts that act as ACS clients for configuration and data retrieval will be provided. Test scripts for unit and integration tests will also be provided.

Support for interfacing to the other subsystems in section 1.1 as needed for commissioning and operation of 16 antennas will be included.

User and technical documentation will be included.

Enhancements to the correlator hardware simulator will be included to incorporate the proposed ‘integrated simulator’

Computer equipment delivered (to coincide with 16-antenna correlator delivery):

- 2 rack-mounted PCs with 2.0+ GHz Opteron processors, CAN controller for CCC and PMC-to-PCI carrier card
- 6 dual-CPU rack-mounted PCs with 2.0+ GHz Opteron processors, 66 MHz bus for CDP. Note that the CPU choice and speed may change, but will stay current of the latest available hardware.
- 4 PCI64-HPDI32A data port cards
- 1 16-port Gigabit switch
- 2 computer racks with UPS and power switches

Status: A reduced set of this equipment was purchase, e.g., 1 CCC, 4 CDP nodes, 1 HPDI32A card, UPSs, no racks nor Gigabit switch.

- **Release 4 Enhanced 16-antenna, one-quadrant correlator**

This release will provide enhanced support for the 16-antenna system. This enhancement will address robustness and more features which satisfy requirements in [Requirements]. Prototyping work on the 32-antenna, 2-quadrant correlator will begin.

Python scripts that act as ACS clients for configuration and data retrieval will be provided. Test scripts for unit and integration tests will also be provided.

Support for interfacing to the other subsystems in section 1.1 as needed for commissioning and operation of 16 antennas will be included.

User and technical documentation will be included.

Computer equipment to be delivered

- 4 dual-CPU rack-mounted PCs with 2.0+ GHz Opteron processors, 66 MHz bus for CDP. Note that the CPU choice and speed may change, but will stay current of the latest available hardware.
- 4 PCI64-HPDI32A data port cards
- 1 computer rack with UPS and power switch

- **Release 5 Support for 32-antenna, two-quadrant correlator**

This release will provide enhanced support for the 32-antenna system. This enhancement will address robustness and more features which satisfy requirements in [Requirements]. Prototyping work on the 64-antenna, 4-quadrant correlator will begin.

- **Release 6 Support 64 antenna, four-quadrant correlator**

  This is the final correlator which will support 33 to 64 antennas. Again the correlator software will be based on the 32-antenna system, but expanded to its full capabilities, i.e., most requirements in [SSR] will be satisfied. The main issues to address at this stage will deal with scaling up of the smaller software system, work which started in Release 1.0.

  Full support for interfacing to the other subsystems in section 1.1 will be included. Final unit and integration test software will be included.

  Final technical and user documentation will be included.

  Computer equipment delivered:

  - 2 rack-mounted PCs with 4 CAN controllers and RS-485 I/O.
  - 18 dual-CPU PCs with 2.0+ GHz Athlon processors, 66 MHz bus. Note that the CPU choice and speed may change, but will stay current of the latest available hardware.
  - 16 PCI64-HPDI32A data port interface cards
  - 2 RS-485 PCI interface cards
  - 2 computer racks with UPS and power switches
  - Spares:1 CAN controller and PMC-to-PCI carrier card, 1 CCC node, 1 CDP node, 1 data port board, 1 Gigabit Ethernet board, 1 RS-485 PCI interface card

- **Post-Release 6 Multiple-quadrant, high-resolution**

  The ALMA correlator, with the use of an optical crossbar switch, can route the same baseband pair to different quadrants. This allows for higher resolution lags, but requires moving the lag data from one quadrant's CDP nodes to another over the CDP network. In order to implement these modes, the following is required:

  - Very high-speed network 10 Gbit or greater, possibly an InfiniBand network (www.infinibandta.org/home)
  - Extremely high-end computers. The extra load on the computers to transfer and process large quantities of lag data is increased by many factors of 10 (or 100?).

1.4 Schedule and Budget Summary

- The total duration of the project is normally 6 years from T0, including 6 months for maintenance support. Should T0 happen after 2002-06-01 still the contract for the correlator subsystem is planned to end on T1=2008-12-31. We plan to use the maintenance support period for final testing and installation.
- The total effort allocated for development of the correlator software is 17 FTE-years for the 6 year project described here. All three positions have been filled at CDR1. An ACA correlator software engineer was hired last year which is funded by ALMA-J.
- The material construction costs estimated for the Correlator Subsystem are 20 K$ for development PCs and workstations, 30 K$ for CCC computers, and 263 K$ for the CDP clusters. A summary of equipment costs appear in Table 5 of section 7.3

- Travel costs are as specified in [Plan].
- The cost of normal development computers are specified in [Plan].

1.5 Document Scope

This Plan represents the terms of a technical agreement between ALMA Computing and the ALMA Software Development Group (SDG) responsible for the Correlator Subsystem. It is subject to configuration control once reviewed. Changes are subject to approval by the Software Problem Report Control Board of the Computing group management.

1.6 Document Evolution

As in [Plan].

1.7 Glossary

The standard ALMA glossary of terms can be found at:

http://www.alma.nrao.edu/development/computing/docs/joint/draft/Glossary.htm

ABM Antenna Bus Master, a real-time computer which controls the hardware devices at the antenna.

ACA ALMA Compact Array, an array of 16 fixed-spaced antennas of 12 and 7 meters with its own correlator.

ACC Array Control Computer, a central computer (or cluster of computers) of the control system which manage the ALMA array.

ACS ALMA Common Software, infrastructure software used by ALMA software subsystems to support the distributed architecture.

ATF Antenna Test Facility, a test facility at the VLA.

AV Audio/Video

CAN Controller Area Network, a multi-drop, deterministic serial interconnect for microcontrollers

CCC Correlator Control Computer, a rack-mounted PC with Ethernet, CAN, RS-232 and digital I/O

CDP Correlator Data Processor, a PC-cluster which obtains raw lags from the correlator and does the FFTs.

CORBA Common Object Request Broker Architecture, an open distributed object computing infrastructure being standardized by OMG.

FDS Fast Data Store, a component of the Archive which distributes the correlator output to the telescope calibration system, the quick look pipeline and to physical data storage.

FIR Finite Impulse Response, the correlator implements bandpass filtering using a digital FIR filter.

LTA Long Term Accumulator, the main computer interface for control and data processing of the correlator hardware.

PCI Peripheral Component Interconnect, a hardware bus designed by Intel and used in PCs and other computers.

PMC PCI Mezzanine Card, a family of low profile mezzanine cards available for various computers busses.

SCC Station Control Card, cards which control station-based electronics in the correlator.

SDG ALMA Software Development Group, the group of subsystems which comprise the Computing IPT.

SI System Integration. Testing of hardware and software for the ATF.

QCC Quadrant Control Card, cards which monitor and control temperatures and power supplies in each correlator quadrant.

1.8 Applicable documents

These documents (unless specified) can be found at:
http://www.alma.nrao.edu/development/computing/docs/index.html

[Plan] ALMA-SW-Draft, *ALMA Computing Plan for Phase 2*, G.Raffi, B.Glendenning

[SSR] ALMA Reviewed Document 11, 2001-MAY-03, *ALMA Science Software Requirements and Use Cases*, Robert Lucas et al.

[Analysis] ALMA-SW-Draft, *Initial Software Analysis*, J.Schwarz et al.

[Architecture] *Software Architecture & High-Level Design*, J.Schwarz et al.

[Practices] ALMA-SW-Draft, *ALMA Software Engineering Practices*, M.Zamparelli

[ACS] ALMA Reviewed Document 16, 2001-SEPT-09, *ALMA Common Software Architecture*, G.Chiozzi et al. Subsystem References

[Requirements] Pisano, J., Hale, A., Scott, S., *ALMA Correlator Software Granular Requirements*, http://almasw.hq.eso.org/almasw/pub/SSR/SoftwareSubsystemsDetailedRequirements/CorrGranReqsV1.4.pdf.

[Test] Shepard, D., *ALMA Software User Test Plan*, http://www.aoc.nrao.edu/~dshepher/alma/testplans/ (2003).

[RTAI] Real Time Application Interface (RTAI) http://mail.aero.polimi.it/~rtai/

[AV] Mungee, S., et. al., *The Design and Performance of a CORBA Audio/Video Streaming Service*, http://www.cs.wustl.edu/~schmidt/PDF/av_chapter.pdf

[ICD] Pisano, J., *Correlator Subsystem Interface Control Document*, http://almasw.hq.eso.org/almasw/pub/CORR/CorrelatorDocuments/CorrelatorICD.pdf (2004).

1.9 References

2 Project Organization

2.1 Organization Interfaces

2.1.1 General Assumptions

- ALMA Computing will oversee the management of the Correlator Subsystem.
- The SSR and HLA groups will be available for commenting on requirement refinements and subsystem designs for the Correlator Subsystem.
- ACS will be utilized as the client-server architecture and provide “middle layer” services.

- The Correlator Subsystem shall follow the guidelines and practices set forth by the Software Engineering group.
- The Correlator Subsystem shall utilize the Integration/Test subsystem for assisting in supplying and executing integration test plans for each release of the Correlator Subsystem software.
- ACS will accept reasonable change requests and new feature requests.

2.2 Group Organization

Figure 3 shows the organization of the software development group for the Correlator Subsystem. The Contact Person is Gianni Raffi and the Subsystem Scientist is Ed Fomalont.

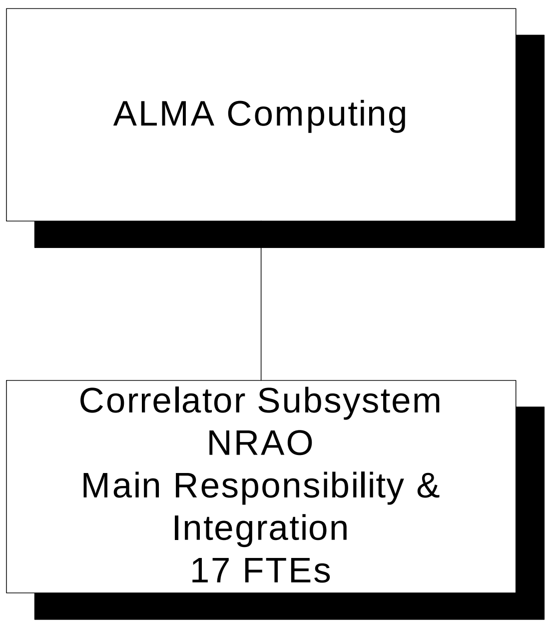

Figure 3 : Organization overview of the Correlator Subsystem

2.3 Roles and Responsibilities

Contact Person: Gianni Raffi	Subsystem Scientist: Ed Fomalont
Project main responsible: Jim Pisano (NRAO)	
Development staff at NRAO for Correlator Subsystem (total 17 FTEs = 3 FTE/year): Jim Pisano at 100% J Perez at 100% R. Amestica at 100% D. Guo at 100% for 4.5 FTEs for ACA Correlator Integration	
Responsibility of NRAO for Correlator Subsystem involves all the Packages shown in section 3.2.	
Packages	**Responsible**

Correlator Control	J. Perez
Data Processor	J. Pisano, R. Amestica
Correlator Hardware Simulator	J. Pisano, J. Perez, & R. Amestica
Test & Integration	J. Pisano, J. Perez, & R. Amestica
ACA Correlator Integration	J. Pisano, D. Guo

Table 1

3 Managerial Process Plans

3.1 Start-up Plan

3.1.1 Estimates

At this point, the estimates in [Plan] are used.

3.1.2 Staffing

The correlator subsystem is fully staffed as of May 2003. Japan will provide 4.5 FTE-years for integrating software between the ACA and NRAO baseline correlators starting in 2005.

3.1.3 Staff Training

On a yearly basis, funds should be available to all subsystem developers for at least a 1-week training session in a technology applicable to the developers' tasks. New programmers will need at least 2 weeks of ACS training as recommended by the ACS group.

3.2 Work Plan

3.2.1 Work Breakdown Structure

The packages for this system are grouped into the 6 categories which are described section 6.3. Required resources for each package group are:

- Correlator Control Packages

  Resources: 4 FTEs

- Data Processor Packages

  Resources: 6 FTEs

- Correlator Station Packages

  Resources: 3 FTEs

- Correlator Simulator Packages

  Resources**:** 1 FTE

- Test and Integration

  Resources**:** 2 FTEs

- TFB Development

  Resources: 1 FTE

- ACA Correlator Integration

  Resources: 4.5 FTEs

3.2.2 Schedule Allocation

Software development has started as correlator hardware is available. Software development on both computer systems (CCC and CDP) will continue in parallel through the remainder of the project.

At this time (CDR 4), no specific critical path can be identified as all work is relevant.

Constraints on the scheduling arise from the deliveries of the correlator hardware. All supporting software must be developed in tandem with the various stages of the correlator hardware and delivered with the correlator hardware.

3.3 Project Tracking Plan

Subsystem project control shall be organized as explained below.

3.3.1 Requirements Management

The requirements for the Correlator Subsystem are generally defined in [Requirements]. They have been refined between CDR2 and CDR3 and satisfy the original SSR requirements. [Requirements] also include software requirements based on the Operations Plan.

3.3.2 Progress Control

Progress control is as specified in [Plan]. The current requirements compliance table can be found in section 7.2.

3.3.3 Quality Control

Quality control is as specified in [Plan].

3.3.4 Communication and Reporting

Communication and Reporting are as specified in [Plan]. User test reports will also be written and provided at CDRs. Teleconferences and the ALMA Twiki along with email are used to communication among groups.

3.4 Risk Management Plan

- Antenna Test Facility

  Concurrent work to support the antenna test facility may have a small impact on the Correlator Subsystem schedule. Delivery of software to support the prototype correlator at the ATF is within the delivery plan and ATF support will be shared among all the correlator developers. Scott Rankin in ITS will assist with support.

- Antenna Delivery Delays

  Delays in the antenna delivery to Chile introduce delays in the commissioning period which delay when the final acceptance is performed.

- Personnel

  As there were not 3 FTEs at T0 and if the total effort remains the same at 17 FTE years, the total duration will extend past the deadline of 2008-12-31 as discussed in section 1.4. The delays in hiring and with the new hires' learning curves taken into account, involving Pisano's support, there is substantial risk that the 17 FTE years will extend beyond the deadline of 2008 by 6 to 12 months.

This potential delay could be alleviated somewhat by hiring extra programmer(s) for a year or two at the end of the project. At that time, tasks would be well-defined and new people could focus on them effectively.

The project time-line has changed such that this personnel risk has diminished somewhat.

- Descoping

  A plan to descope features is needed if certain releases can't be met. The SSR provides guidance for feature prioritization.

- Integration testing with correlator hardware in Chile

  Once the first quadrant is shipped to Chile for supporting the first 16 antennas, it may be difficult to test out the full 4-quadrant system in CV. This will affect testing. This risk can be somewhat mitigated by providing simulators for the correlator hardware. Testing of all 4 quadrants can occur in Chile, but the hardware delivery schedule does not exactly coincide with the software delivery schedule, e.g., delivery of the fourth quadrant to Chile is planned for Q4 2009, which is after the Q4 2008 software contract termination date. Thus testing of the complete system within the timeframe of this software contract cannot be done.

  It is to be accepted by B. Glendenning and G. Raffi that final installation and testing of the correlator subsystem software will continue into Q4 2009.

- Hardware Risks

  Other than the delivery mismatch of hardware and software deliveries, I do not foresee any software delays due to delayed correlator hardware deliveries.

- Tunable Filters

  The tunable filter enhancement will require approximately 1 FTE of software development time. It may be possible for the TFB group to assist with the software development to lessen the 1 FTE.

3.5 Project Termination Plan

Project termination is as specified in [Plan].

4 Technical Process Plans

4.1 Development Model

Correlator Subsystem Start (**T0**) As defined in [Plan], T0 will be 2002-06-01
Internal Design Review (**IDR**) December 2002
Preliminary Design Review (**PDR**) (T0+6 months) March 2003
Critical Design Reviews (CDR1 – 3) (T0+10 months and yearly afterwards)
CDR dates are July 2003, July 2004 and July 2005.
R0 (2003-05-01): 2-antenna prototype correlator development support.
R1 (2003-10-01): 2-antenna prototype correlator support delivered to SI (prototype correlator

ready to ship to AOC 2004 Q1)
R2 (2004-10-01) 2 antenna prototype correlator**,** 16 antenna, single quadrant correlator development support. Correlator hardware simulator
R3 (2005-10-01) Enhanced support for the 2-antenna correlator, prototyping support for the 16-antenna, one-quadrant correlator
R4 (2006-10-01) Enhanced 16-antenna, one-quadrant correlator
RR (Readiness Review) (T1-12 months) The RR date is May 2007.
R5 (2007-12-01) Support for 32-antenna, two-quadrant correlator
PAR (Preliminary Acceptance Review) (2007-12-01) The PAR date is December 2007. Correlator staff shall be available in Chile to perform commissioning tests, with the support of the ALMA site operations group. Correlator personnel will be responsible for acquiring and shipping on time all the computing equipment needed in Chile.
R6 (2008-12-31) Support 64 antenna, four-quadrant correlator
Support Completion (T1=2008-12-31, normally T0+6 years) This Phase normally overlaps with the Subsystem Upgrade (4 years) which is not covered by this document and will imply a new Development Plan and a new Agreement. Note that this will extend into Q2 2009 due to the correlator delivery schedule and required testing time of 3 – 6 months.

Table 2 – Development Model

4.2 Release Issues

This section identifies any issues that arose during the releases.

- R0 No issues arose for this release
- R1
    - Some miscommunication regarding the publication of integration event data and problems with starting and stopping of spectral data to the BulkStore arose during testing. These were relatively minor problems which were resolved in R1.1.
    - Delivery of software to support the SI testing occurred in mid-February, but wasn't used until June (at least). Keeping the correlator in Charlottesville through June would have assisted further development for R2. Test support for the tests will interfere with R2 deliverables to some degree which cannot currently be defined.
- R2
    - There were substantial delays in the integration due to difficulties with the RTAI installation used by ITS.
    - User tests were not performed and no report was issued.
    - R2.1 integration went well. The problems encountered in R2.0 were resolved and only minor bugs were encountered during the integration.

- R3
  - Features planned for R3.0 were delivered but could not be fully tested in a end-to-end fashion due to problems with other subsystems.
  - R3.1 Feature enhancements for R3.1 were postponed as management requested that a version of RTAI-independent correlator software be developed. This non-RTAI capability was not completed because a real-time robustness effort was undertaken which drew needed resources.

4.3 Methods and Tools

The real-time Linux variant, RTAI will be utilized as a real-time micro-kernel for the CDP and CCC computers. The Correlator system will be written in C++, Python, and Java.

4.4 Infrastructure

Section 7.3 shows the projected costs of this equipment. Note that dates are for the beginning of the release phase for which the equipment is needed. Section 1.3 details the delivery schedule of the required computer equipment. In general, all computer equipment will be purchased 6 – 12 months in advance of its delivery.

4.5 Acceptance Plan

4.5.1 Acceptance Tests

Acceptance tests will be consistent with the *ALMA Software User Test Plan* [Test] and will consist of:

- Unit tests of individual packages outlined in section 3.2.1. These unit tests will test the ACS interfaces of each package group, i.e., Correlator Control Packages, Data Processor Packages, and Correlator Station Packages before they go to integration testing.
- Performance tests of real-time components for the CCC and CDP packages
- System tests where the correlator subsystem interfaces to other subsystems

5 Supporting Process Plan

5.1 Configuration Management

The configuration management processes as described in [Practices] are applicable.

5.2 Validation

System integration test plans for the Correlator subsystem are written by the ITS (Integration, Test, & Support subsystem) for each release.

5.3 Documentation

5.4 Quality Assurance

As is defined in [Practices].

5.5 Reviews

No other reviews outside of the PDR and CDRs are required.

5.6 Problem Resolution

The existing ALMA SPR system as described in [Practices] shall be used.

5.7 Process Improvement

At this time, no processes can be identified for improvement.

6 Software Description

6.1 Software External interfaces

6.1.1 ACS Interfaces

- Services and core components used by Correlator Control, Correlator Station and Data Processor Packages include Container-Component model, Error, Logging, Alarm, Time, Process/Distributed Object life-cycle management, CORBA middleware, and Audio/Video streaming service (encapsulated in the BulkData service).

6.1.2 Control Subsystem

- Configuration of correlator hardware, CCC and CDP
- Synchronization with other telescope hardware
- Monitoring interface of correlator hardware, CCC and CDP
- Provide real-time antenna status information which is used for antenna-based blanking at the correlator
- Provide geometric delay model parameters
- Provide water vapor radiometry values and correction coefficients from the telescope calibration subsystem.
- Provide Telescope Configuration Data Base with API to track current hardware.

6.1.3 Archive Subsystem

- The raw science data blocks created by the CDP will be published via the CORBA A/V streaming service (encapsulated in the BulkData service of ACS) to which the BulkReceiver (Archive) subscribe.
- Monitor data storage for CCC and CDP (via Control)

6.1.4 Observing Tool Subsystem

- Supply the OT with current correlator configuration capabilities
- Provide correlator configuration validation capability

6.1.5 Data Capture (Offline Subsystem)

- Correlator will send integration and sub-integration durations and times per subscan and subarray.
- Correlator will pass sub-scan configuration information from Control to DataCapture.

6.2 Software Design

The result of Phase 1 work in terms of High Level Analysis and Architecture is given respectively in [Analysis] and [Architecture]. This is applicable to Subsystems and represents the start point for the Subsystem design activity.

The Subsystem Concept is described in section 7.4.

6.3 Packages

Packages are grouped by category of correlator control, data processor, simulator, correlator configuration validator, and test and integration.

- Correlator Control Packages

  These packages deal with the configuration, control and monitoring aspects of the correlator.

  - ACS Interface
  - Monitor
  - Geometric Delay
  - Command Dispatcher / Configure Sub-scan
  - Tunable Filter
  - CAN Interface
  - Array Time
  - Maintenance
  - CAN Commands
  - Subarray Management

- Data Processor Packages

  These packages deal with the configuration, monitoring and operation of the correlator data processor computer system.

  - Array Time
  - CDP Master and Compute Node
  - Data Publisher
  - Monitor
  - Maintenance
  - Cluster Admin
  - Spectral Processing
  - Lag Processing
  - HPDI 32
  - Tunable Filter
  - Residual Delay
  - Atmospheric Phase Correction

    - Double side band receivers
    - CDP Configuration
    - Subarray Configuration
    - TE Scheduler
    - Data blanking
- Simulator

  These packages simulate the configuration, control, monitoring and raw lag output of the correlator hardware. The purpose of the simulator will be to allow for subsystem and integration testing when the correlator hardware is not available.

    - LTA configuration
    - Station cards configuration
    - LTA monitoring
    - Station cards monitoring
    - Quadrant Control Card commands
    - Quadrant Control Card monitoring
    - Raw lag output
    - Interface to the Shared Simulator
- Correlator Configuration Validator
- Test and Integration

  Test and integration are listed as packages which need implementation and span across the 4 package groups.

- ACA Correlator Integration
    - Integration of correlator hardware configuration
    - Integration of correlator data processing configuration
    - Integration of correlator configuration validation
    - Integration of correlator output data formats
    - Testing

6.4 Interfaces between Packages

The interfaces between Correlator Subsystem packages are described in [ICD].

6.5 Integration of Packages

Procedures to integrate Packages into a Subsystem, including logistic aspects are described in document TBD.

7 Attachments

7.1 General Phase 2 Planning Model

These review and release dates come from [Plan]. They are matched to the proposed delivery dates of the correlator hardware.

Reviews	Date	Software Releases	Date	Correlator Hardware	Date (ready to ship)
IDR	2002-12-10				
PDR	2002-03-15	R0	2003-03-20		
CDR 1	2003-07-10	R1	2003-10-01	2-ant. proto.	2003-8-29
CDR 2	2004-07-10	R2	2004-10-01		
CDR 3	2005-06-31	R3	2005-10-01		
CDR 4	2006-05-01	R4	2006-10-01	32-ant. 2 quad.	Q1 2007
RR	2007-05-01	R4.1	2007-05-01		
PAR	2007-12-01	R4.1	2007-05-31		
		IR 5	2007-12-01		
		IR 6	2008-12-01	64-ant. 4 quads.	Q2 2009

Table 3

7.2 Requirements Compliance Table

The requirement references are from [Requirements] which derive from the SSR requirements.. Requirements in the SSR column in **bold** refer to the requirements from the Operations Plan in [Requirements]. The ‘Release’ column only shows partial features to be implemented each release. An iterative development effort is planned such that each release will contain incremental functionality for each package. For example, Release 1.0 will have enough of each package to support the 2-antenna prototype correlator for SI testing. Releases 4.0 & 5.0 will satisfy 16- and 32-antenna systems, and release 6.0 for the 64-antenna system. Further details of the features for each package are provided subsequent CDRs.

Package	Feature	Short Description	SSR Number	Release	Status (N,P,C)
CCC Correlator Subscan Configuration	Correlator configuration	Configure the subscan parameters of LTA. Provide validity information about correlator configurations.	2.1-R7 2.1-R8 2.1-R10 2.2-R1 2.2-R4 2.3-R8 2.3-R12 3.0-R7 3.0-R8, OPS-8.1.1 OPS-8.1.2 OPS-8.1.3 OPS-8.1.5	R2: 2 correlator modes for 1 baseline R3: TFB configuration 2-antenna, 4 basebands 2 Subarrays R4: 16-antennas, 4 basebands 2 subarrays R5: 32-antennas, 4 basebands, 2 subarrays R6: 64-antennas, 4 basebands, 4 subarrays	R2: C R3: P
CCC CAN Commands	Correlator Configuration	Control of LTA& SCC via command protocol	2.2-R2 2.3-R2 OPS-4.1.2 OPS-8.1.1 OPS-8.1.2	R2: Basic M&C cmds for test & operation of 2-ant. Prototype R3: 1 quadrant, 16-antenna M&C cmds prototypes R4: 1 quadrant, 16-antenna M&C cmds R5: 2 quadrant, 32-antenna M&C cmds R6:4 quadrant, 64-antenna M&C cmds	R2: C R3: C
CCC Array Time	Configuration synchronization & time stamps	Provide ACS::Time for monitor data and correlator configurations start times. TE access and synchronization with	1.0-R6 2.1-R7 2.2-R4 2.3-R1	R2: Configuration start times & time stamps, synchronization.Simulate TEs & TE I/F R3: Full support of ArrayTime setting protocol R4: Resolve any outstanding issues R5: R6:	R2: C R3: P

Package	Feature	Short Description	SSR Number	Release	Status (N,P,C)
CCC Monitor	Correlator Monitoring	ACS Property monitoring interface using QCC	1.0-R10 2.3-R2 5.0-R1 5.0-R4 7.3-R2 OPS-5.1.2 OPS-8.1.10 OPS-8.1.18	R1 Simple monitoring at single rates. R2: Implement QCC interface R3: LTA/SCC monitor,TFB monitor R4: 1 quadrant, 16 antenna support R5:2 quadrant, 32 antenna support R6:4 quadrant, 64 antenna support	R2: C R3: C
CCC Tunable Filter	Tunable Filter Board Support	Configure tunable filters	COR-T16	R3: Basic TFB support R4:Enhancements R5: Diagnostics support R6: Final operational support	R3: C
CCC Subarray Management	Subarrays	Provide support for subarrays	2.1-R8 OPS-8.1.5	R2: No support R3: 2 configs per subarray for 2 subarrays. R4: 4 subarray support R5: 2 configs per 4 subarrays R6: Final operational support	R3: N
CCC ACS Interface	ACS Interface	Provides ACS Interface layer to device-dependent code	1.0-R3 2.1-R1 2.1-R2 2.2-R2	R2: Interface for M&C, notification channel, AV streams R3: Control Master Component support R4:Changes to ACS I/F updates R5:Changes to ACS I/F updates R6:Changes to ACS I/F updates	R2: C R3: C

Package	Feature	Short Description	SSR Number	Release	Status (N,P,C)
CCC Maintenance	Maintenance	Provide correlator and CCC maintenance.	OPS-4.1.6 OPS-4.1.9 OPS-4.1.10	R2.1 Cable training for proto. correlator, Block read/write tests R3: Cable training baseline correlator, Correlator HW tests Reset R4: 1 quadrant, 16 antenna diagnostics R5:2 quadrant, 32 antenna diagnostics R6: 4 quadrant, 64 antenna diagnostics support	R2,1 C R3: P
Configure Data Processing	CDP Configuration	Set data processing options for CDP	2.1-R10 2.1-R11 2.2-R1 2.3-R6 2.3-R8 2.3-R9 2.3-R10 3.0-R7 3.0-R8OPS-8.1.1 OPS-8.1.2 OPS-8.1.3 OPS-8.1.5	R1 & R2: Configuration for 2 corr. modes & data processing options R3: TFB configuration 16-antenna, 4 basebands 2 subarrays R4: 1 quadrant 16 antennas R5:2 quadrant 32 antennas R6:4 quadrant 64 antennas	R1: C R2: C R3: P
CDP Monitor	CDP Monitoring	ACS Property monitoring interface	1.0-R10 2.3-R2 5.0-R1 5.0-R4 7.3-R2 OPS-5.1.2 OPS-8.1.10 OPS-8.1.18	R1 & R2 Simple monitoring at single rates. R3: CDP computer monitoring, temperatures, voltages, fans, real-time task usage. R4: Enhancements, h/w change support R5:Enhancements, h/w change support R6: Final operational implementation	R1: C R2: C R3: N

Package	Feature	Short Description	SSR Number	Release	Status (N,P,C)
CDP Maintenance	Maintenance Cluster Admin.	Maintenance of software & hardware. Cluster administration	OPS-4.1.6 OPS-4.1.9 OPS-4.1.10	R2: Manual cluster administration R3: Remote booting, 5-node CDP R4: Enhancements for 9-node cluster R5: Enhancements for 17-node cluster R6:Deliver to operations w/ redundant master	R2: C R3: N
CDP HPDI 32	Raw Lag Data Processing	Real time interface to data ports to obtain raw lags	1.0-R9 2.3-R3 2.3-R4	R1.0 Support for 32 MB/sec R2: 16 ms dump support R3: Minimal TFB support2 subarrays R4: Full TFB support, 2 subarrays R5: 32 antennas, 4 subarrays R6:64 antennas, 4 subarrays	R1: C R2: C R3: C
CDP Master and Compute Node	Raw Lag Data Processing	Translates external commands to internal commands	1.0-R9 2.3-R3 2.3-R4 2.3-R6 OPS-8.1.1 OPS-8.1.2 OPS-8.1.3	R1.0 Basic Support for 2-node cluster. R2-3 Support 5-mode cluster R4: Support 9-node cluster R5:Support 17-node cluster R6:Enhancements to full cluster	R1: C R2: N R3: N
CDP Lag Processing	Raw Lag Data Processing Atmospheric Phase Correction Double side band receivers	Convert raw lags to spectra according to data processing configuration, handle data blanking, correct for WVR	1.0-R9 2.1-R7 2.1-R10 2.3-R1 2.3-R2 2.3-R3 2.3-R4 2.3-R6 2.3-R7 2.3-R11 OPS-8.1.1 OPS-8.1.2	R1.0 Basic support for 2 auto- & cross-corr. modes R3: Initial WVR corrections, blanking. R4: Enhanced blanking R5: Enhanced WVR R6:Side-band separation	R1: C R2: C R3: P

Package	Feature	Short Description	SSR Number	Release	Status (N,P,C)
			OPS-8.1.3		
CDP Lag Processing	Performance analysis	Analyze lag to spectra data processing	Internal requirements	R2.0 Initial RMA R3: Simple timing tests R4: Full analysis with TFB on Opteron	R2: C R3: C
CDP Tunable Filter	Raw Lag Data Processing	Process data from tunable filters		R2: Minimal correlator HW test support R3: Basic TFB support R4: Enhanced modes R5: Continued enhanced modes R6: Final operation versions	R2: C R3: C
CDP Residual Delay	Raw Lag Data Processing, Delay Control	Performs fine delay adjustment on spectra	2.1-R10 OPS-8.1.1 OPS-8.1.2 OPS-8.1.3	R 2.0 Initial framework R3: Receive delay events R4: 1 quadrant, 16 antennas R5: 2 quadrants, 32 antennas R6: Full implementation, 64 antennas, 4 subarrays	R2: C R3: C

Package	Feature	Short Description	SSR Number	Release	Status (N,P,C)
CDP Data Publisher	Raw Lag Data Processing	CORBA A/V Service for raw spectra to be sent to Archive.	1.0-R8 1.0-R9 2.3-R3 2.3-R4 2.3-R5 2.3-R6 2.3-R11 7.2-R1 OPS-5.1.2 OPS-8.1.1 OPS-8.1.2 OPS-8.1.3	R1.0 Support for Python client using CORBA NC R2 VOTables to Archive, DataCapture framework R3: XML + binary. Use ASDM from UML to DataCapture R4: Support for 1 quadrant 16 antennas R5:Support for 2 quadrants 32 antennas R6:Support for 4 quadrant 64 antennas	R1: C R2: C R3: C
CDP ACS Interface	ACS Interface	Provides ACS Interface layer to device-dependent code	1.0-R3 2.1-R1 2.2-R2	R1, R2: Interface for M&C & publish-subscribe services R3: Updated delay & blanking NC R4:Changes to ACS I/F updates R5:Changes to ACS I/F updates R6:Changes to ACS I/F updates	R1: C R2: C R3: P
Correlator Hardware Simulator	Control Interface Simulator	Provides configuration and control simulation of correlator hardware via CAN commands	Internal requirements for integration testing	R2.0 basic supportR 3 - R6: Enhancements	R2: C R3: C
Correlator Hardware Simulator	Monitor Interface Simulator	Provides monitor simulation of correlator hardware	Internal requirements for integration testing	R2.0 Basic QCC data 3 - R6: Enhancements	R2: C R3: C
Correlator Hardware Simulator	Raw lag output Simulator	Generate raw lag data based on configuration	Internal requirements for integration testing	R2.0 basic features 3 - R6: Enhancements	R2: C R3: C

Package	Feature	Short Description	SSR Number	Release	Status (N,P,C)
Configuration Validator	Configuration Validator	Static analysis of correlator configuration	2.1-R10 2.1-R11 2.2-R1 2.3-R6 2.3-R8 2.3-R9 2.3-R10 3.0-R7 3.0-R8 OPS-8.1.27	R1 Done. R2: Adapt to config changes R3: Adapt to TFB changeschanges R4: Update as configuration changes R5: Update as configuration changes R6:Deliver final operational version	R1: C R2: C R3: C
non-RTOS	RTOS independent version	Run correlator software on pure non-RT Linux	Internal requirements for integration testing	R4.0 All RTAI-dependencies removed	

Table 4 - Compliance Matrix

7.3 Computer Equipment Costs

This table provides guidelines for the various equipment expenses foreseen for the Subsystem. Of course these estimates may change with time, but they try to distribute the allotted amount in [Plan] among the various hardware components needed for the Subsystem.

Release	CCC Cptrs	CAN Cards	CDP Nodes	Data Port Cards	Gigabit Switch	Rack	UPS	KVM/ Monitor	Misc Cost	CCC Cost	CDP Cost	Total Cost
1	2	1	2	1	0	0	1	0	$1,500	$8,000	$10,500	$20,000
2	1	1	4	4	0	0	2	2	$7,000	$4,500	$30,000	$41,500
3	2	2	8	4	0	1	1	1	$6,500	$9,000	$42,000	$57,500
4	0	0	8	4	0	1	0	0	$3,000	$0	$42,000	$45,000
5	0	0	0	0	0	0	0	0	$0	$0	$0	$0
6	2	2	18	4	1	2	8	4	$28,000	$9,000	$72,000	$109,000
Spares	1	1	3	3	1	0	0	0	$2,000	$4,500	$22,500	$29,000
Totals	**8**	**7**	**43**	**20**	**2**	**4**	**12**	**7**	**$48,000**	**$35,000**	**$219,000**	**$302,000**

Table 5 Computer Equipment Costs

7.4 Subsystem Concept

The correlator hardware follows the model of "configure-and-run" which is repeated as needed for an sub-scan. Referring to Figure 1, this process is broken down into the following steps:

- For a specified subarray, which consists of 1 – 64 antenna inputs to the correlator hardware:

- Prepare for acquiring data involving the reception of configuration information from the ACC. Set up internal data structures describing the sub-scan like correlator mode, dump, integration and sub-scan durations and data processing parameters. These configuration commands will be time-tagged an sent to the CCC well in advance of when they need to be applied.
- Configure the correlator hardware (LTA, station cards and FIR filter cards) at a specific timing event in preparation for an sub-scan.
- Obtain initial geometric delay model information as needed and applying initial delay information to the various hardware components at the specific timing event
- Start integrations on a specific timing event
- Retrieve raw lag results from the LTA
- Blank antenna data based on antenna blanking event channel
- Process correlator results e.g., apply FFTs, fine delay adjustments, application of WVR data, double side-band separation, etc.
- Update the geometric delay model and apply to correlator hardware components as needed
- Transmit the spectral results to the Archive data distributor.
- Provide channel average data on periodic basis
- Transmit channel average results to the Archive data distributor.
- Transmit MainTable data to DataCapture.
- Repeating the above 5 steps until integrations are stopped as defined by the sub-scan duration or by an abort command sent by the ACC. Note that configurations, start and stop observing commands can be queued as the CCC will support time-tagged commanding.