Atacama
Large
Millimeter
Array

64-Antenna Correlator Specifications and Requirements

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Table of Contents

Revision History:

2016-Dec-05: Initial Issue

2016-Dec-19: Incorporate Baudry and Escoffier comments

2016-Dec-21: Incorporate additional Baudry comments

2016-Dec-30: Incorporate Amestica and Escoffier comments

2017-Nov-28: Add Phase 1 and Phase 2 descriptions and Phase 0 tables. Update block diagram description. Fix typos.

2017-Dec-04: Fix typos in Table 2a, modes 6, 25 and 58

2017-Dec-11: Incorporate Escoffier's comments

2017-Dec-13: Incorporate Saez's comments

2017-Dec-18: In all mode tables, change "spectral resolution" to "channel width". Per Crystal Brogan, this is more in agreement with the nomenclature used by astronomers. Add a note that actual spectral resolution will be about a factor of 2 coarser due Hanning smoothing.

2018-Jan-08: Change the note, below Table 1, pertaining to the number of lags. Update the doc number in the header. Update the block diagram. Remove note about VLBI compatibility in Table 4a.

2018-Jan-11: Corrected typo on page 10, paragraph 4 ("tunable"). Added ALMA Document number.

2018-Jan-19: Corrected typo on table 1: "32768 spectral points" becomes 65536 spectral points. Clarify sample format on table 1 for phase 1 and phase 2.

2018-Feb-05: Address **RIDs 857, 859, 860, 861** posted by Gie Han. Added AD06. Modified version on AD04 and AD05. Update document number on AD03

2018-Feb-015: In response to **RID-868,** modify entire document to make it include only specifications for phase 1. Change the sensitivity column in Tables 2, 3, and 4 to take into account the sensitivity degradation of the 3-bit sampler in the IFsystem in response to **RID-871**. Modify Table 1 caption in response to **RID-869**. Change "spectral windows" to "basebands" in response to **RID-873**. Re-write the section on the High Time Resolution feature in response to **RIDs 882, 883 and 893**. Partly prompted by **RID-891**, add a paragraph stating that sub-array and multi-resolution modes are unchanged and provide details.

2018-Feb-023: In response to comments by Crystal Brogan, modify note 3 in mode tables 2 and 3 were modified and make a slight change to block diagram (green text). Update TDM sensitivity per RID-871.

2018-Mar-013: Corrected document title referenced in AD-04. Updated date and title.

ALMA CORRELATOR UPGRADE SPECIFICATION

1 Introduction and Summary

This document describes phase 1 of the ALMA 64-Antenna correlator upgrade. The ALMA correlator is a lag correlator with a digital filter bank in the input section of the system that permits it to operate as a digital hybrid correlator (FXF). The system can also be operated in a wideband time division mode (XF).

Overall system specifications for the ALMA correlator can be seen in Table 1.

Table 1. ALMA Correlator Specifications

Item	Specification
Number of antennas	64
Number of baseband channel inputs per antenna	8 (2 orthogonal polarizations x 4 basebands)
Input sample format	3-bit, 8-level at 4 GSample/s per baseband channel
Correlation sample format	2 bit, 4 level and 4 bit, 16 level; Nyquist and twice Nyquist
Maximum baseline delay range	300 km***
Hardware cross-correlators per baseline*	262,144 leads + 262,144 lags
Hardware autocorrelators per antenna*	262,144 (2048 lags/sub-band x 32 sub-bands x 4 basebands)
Typical performance in digital hybrid modes	65536 spectral points provided for each pair of baseband inputs**
Product pairs possible for polarization	HH, VV, HV, VH (for orthogonal H and V)

* 62.5 MHz correlators (125 MHz clock rate). In TDM, divide by 32 to get number of equivalent 2 GHz correlators.
**Resulting in between 2048 to 65536 spectral points across the baseband spectrum depending on polarization mode, number of bits and oversampling ratio. See tables 2, 3 and 4 for a detailed description of the available permutations.".
***the design of the current correlator can also accommodate 300 km baselines, but this was not included in the original specification. This capability refers only to the amount of delay memory; using longer baselines may require new approaches to updating delays due to the high delay rates for long baselines.

The ALMA correlator evolved from an initial system design (described in ALMA memos 166 and 194) with a pure lag architecture incorporating simple FIR digital filter cards (described in ALMA memos 204 and 248) to a design implementing a digital hybrid correlator with the incorporation of 32-element digital filter bank cards.

The fundamental change to the original design, the replacement of the digital filter card with a tunable filter bank card, is based on the design philosophy of the proposed '2nd Generation Corelator' system (and is described in ALMA memo 476). The

use of a 32-element filter bank instead of a single digital filter has the effect of increasing the performance of the system by factors of up to 32 in spectral resolution.

A single wideband time-packet or time-division mode of the original system design has been retained in the operation of the correlator to provide high time resolution where this parameter is of highest importance.

The ALMA correlator upgrade evolved from a need to provide ALMA with additional processing power approximately 15 years after the start of the original design. The upgrade uses the original infrastructure (racks, power, clock distribution, cooling). It replaces cards in the data chain with new cards that can run at 250 MHz (internally generated from the provided 125 MHz). Additionally, it replaces the original correlator chip with one that has 32 times the processing power (8 times as many lags per antenna pair and 4 times the number of antenna pairs) and that can run at 250 MHz. The resulting system produces 8 times as many spectral points. The 250 MHz capability is a feature to enable future enhancements.

2 Applicable and Reference Documents

21 Applicable Documents List (ADL)

The following documents, with the revision in force as of the date of this specification, form part of this SOW. In the event of conflict between the documents referenced here and this document, this document shall take precedence.

No.	Document Title	Reference
AD 01	ALMA Product Assurance Requirements	ALMA-80.11.00.00-001-D-GEN
AD 02	ALMA System Electromagnetic Compatibility Requirements	ALMA-80.05.01.00-001-B-SPE

AD 03	ICD between Site and Correlator	ALMA-20.01.02.00-60.00.00.00-A-ICD
AD 04	ICD between Back-End and Correlator	ALMA-50.00.00.00-60.00.00.00-C-ICD
AD 05	ICD between Correlator and Computing Correlator Software	ALMA-60.00.00.00-70.40.00.00-E-ICD
AD06	ALMA System Technical Requirements	ALMA-80.04.00.00-005-C-SPE

22 Reference Documents List (RDL)

No.	Document Title	Reference
RD 01	ALMA Project Plan, Version II	Dated September 23rd, 2004
RD 02	ALMA Design Reviews - Definitions, Guidelines And Procedures	ALMA-80.09.00.00-001-D-PLA
RD 03	ALMA Product Tree	ALMA-80.03.00.00-001-R-LIS

23 Definitions, Abbreviations and Acronyms

AD	Applicable Document(s)
ADL	Applicable Documents List
ALMA	Atacama Large Millimeter Array
AOS	Array Operations Site
CCC	Correlator Control Computer
CDP	Correlator Data Processing computer
Corr	Correlator
CPLD	Complex Programmable Logic Device
CVS	Concurrent Versions System (a revision control system)
DRX	Digital Receiver Card
DTS	Digital Transmission System
ESO	European Southern Observatory
FDM	Frequency Division Multiplexing
FPGA	Field Programmable Gate Array

FXF	Fourier-transform, correlate, Fourier Transform (a type of correlator architecture)
ICD	Interface Control Document
IPT	Integrated Product Team
JAO	Joint ALMA Office
LAB	Laboratoire d'astrophysique de Bordeaux
LTA	Long Term Accumulator
NRAO	National Radio Astronomy Observatory
NTC	NRAO Technology Center
OSF	Operations Support Facility
QCC	Quadrant Control Card
RDL	Reference Document(s) List
SCC	Station Control Card
SOW	Statement of Work
TB	AOS Technical Building
TFB	Tunable Filter Bank
TDM	Time Division Multiplexing
XF	Correlate, Fourier Transform (a type of correlator architecture)

3 System Block Diagram

A block diagram of the ALMA correlator can be seen in Figure 1. Changes resulting from the upgrade are highlighted in green. This figure also includes some details of the ALMA digitizers and the DTS transmission system. Although these components of ALMA are not part of the correlator, they are shown here for clarity.

The input stage of the correlator is the tunable filter bank card. This stage is driven by the output of the ALMA DTS receiver/demux card which recovers the 3-bit samples generated by the ALMA digitizer sent via optic fiber from the remote antennas over the ALMA Digital Transmission System. The filter-bank card can be configured as 32 digital filters with either 62.5 or 31.25 MHz bandwidth, depending on selected pre-calculated taps in the last stage of the decimation filter. The center frequency of each filter, as well as the phase of the digital LO associated with each filter, is independently tunable.

The station card has several functions with the main ones being implementing bulk delay for geometric delay adjustment, implementing delays

required by some modes, routing desired filter card outputs to correlator inputs and providing the “corner turn” for the TDM modes. Programming in the station cards determines how the 32 filter outputs of the filter card are processed in the correlator system.

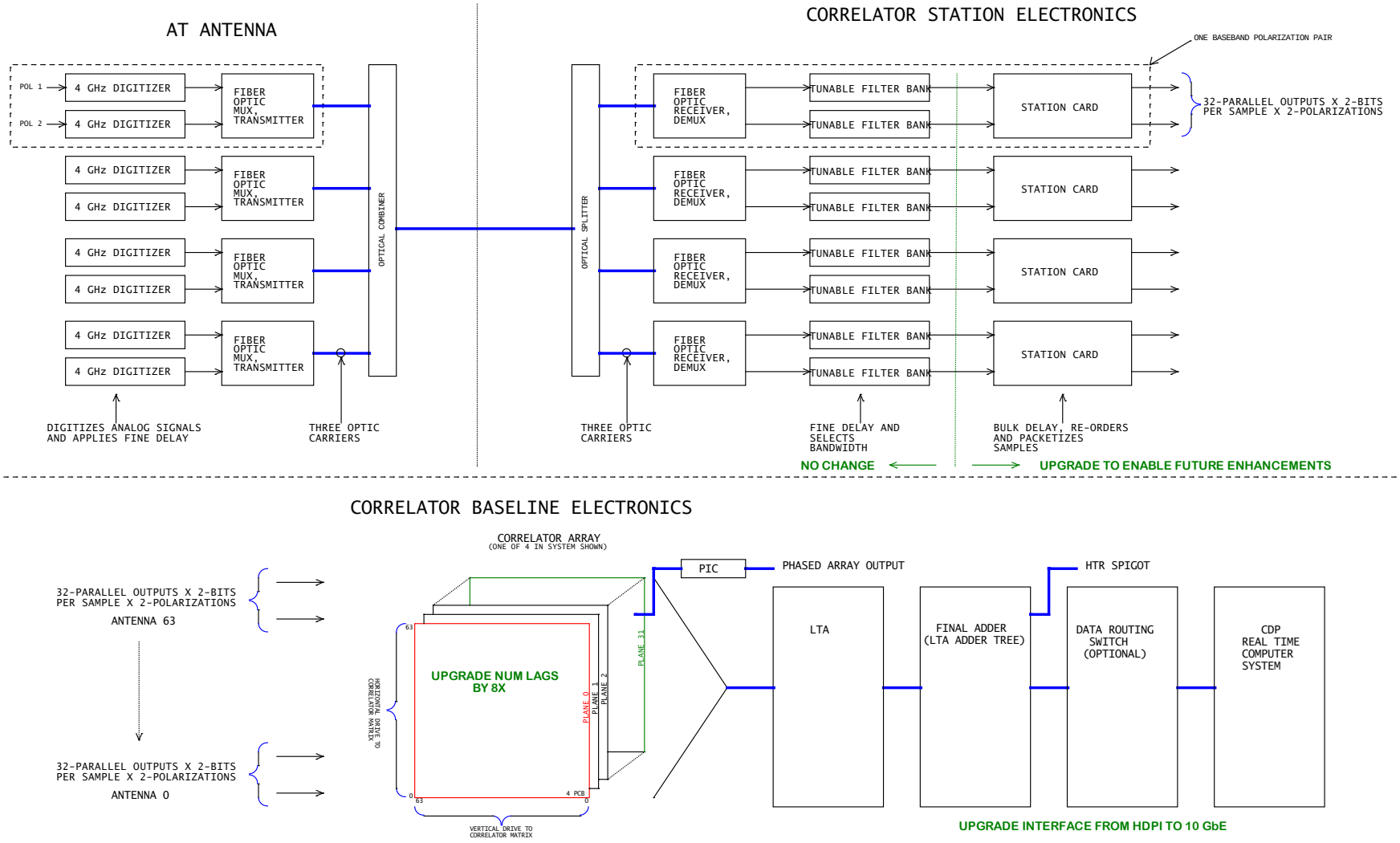

Figure 1. Correlator Upgrade Phase 1 Block Diagram.

The correlator portion of the system consists of 32 correlator planes each implementing a 64-by-64 correlation matrix. (Each correlator plane is implemented in one correlator card.) When samples from all 64 antennas in the ALMA main array drive this matrix (both axes), autocorrelations are produced on the matrix diagonal and cross correlations are produced elsewhere (with leads on one side of the diagonal and lags on the other).

The LTA (Long Term Accumulator) subsystem seen in Figure 1 takes short, 1 to 16 msec, integrations output by the ALMA custom correlator chips and provides long term integration for them, up to 1.008 seconds. The results of these integrations are sent to the LTA adder tree, also known as the Final Adder. In time division modes (TDM), the adder tree adds the results from all the correlator planes. (This is not necessary in frequency division modes (FDM).) The Final Adder also packetizes the data for transmission to the Correlator Data Processor computers. The packets may be routed directly to the Real Time Computer system or a Data Routing Switch may be used.

The ALMA correlator is designed in 4 essentially identical quadrants. Each quadrant processes the output of two of the eight baseband channel outputs of the array. For polarization observations, the two baseband channel outputs processed in a quadrant must be of opposite polarizations.

For the phase 1 upgrade, all cards in the data path except the Data Receiver and Tunable Filter Bank Cards are upgraded. The upgraded cards are programmed to operate at 125 MHz to process 2 GHz chunks of spectrum in each quadrant, just like the original correlator. They will be designed to operate at twice this rate to enable future enhancements. The main difference in performance will be an 8-fold increase in spectral resolution.

Note that the bandwidths quoted in this document are exactly half of the sample rate. This is a common practice in radio astronomy, typically resulting in nice round numbers for processed bandwidth. However, in FDM modes, 6% of the bandwidth is lost due to the need to provide a guard band to prevent aliasing and good phase response.

4 Sub-system Description

4.1 Data Receiver and Tunable Filter Bank Card

The purpose of the Digital Receiver Card (DRX) is to receive the samples transmitted on fiber from each antenna via the 1:12 optical splitter in the AOS Fiber Room. In addition the Data Receiver Card demultiplexes the data stream so that subsequent signal processing can occur at a lower clock rate.

The Tunable Filter Bank card has two primary purposes. First, it inserts delays, with a resolution of one 250ps sample, into the data stream to compensate for the geometric delay of the array. Second, it divides the 2 GHz input spectrum into up to 32 subchannels. The bandwidth of each of these subchannels can be 62.5 MHz or 31.25 MHz. Each of the subchannels can be placed anywhere within the 2 GHz input band by setting a digital local oscillator frequency.

4.2 Station Card

Each Station card provides two 4-millisecond RAM buffers, one for each of two filter card outputs (that is, each buffer holds approximately 4 milliseconds of samples at the full 8 GHz sample rate of a single baseband channel output). A station card provides several basic functions in the correlator:

- Provides bulk storage of the geometric delay adjustment
- Provides a versatile cross bar function between the filter card output and the correlators
- Provides lag generation for high frequency resolution modes
- Generates time packets of samples in time division mode

The two basic modes of the station card reflect the two operational modes of the ALMA correlator, TDM and FDM. Most observations will use the high frequency resolution digital hybrid FDM configuration. In these cases, the input to the station card from a filter card(s) consists of from 1 to 32 separate bands each with a 125 MHz clock rate (either Nyquist sampled or twice Nyquist sampled for the oversampled modes of table 2, 3, and 4). The other operating mode of the correlator, TDM, is used in high time resolution observations. In this mode, the filter cards provide a pass through function and the station card input is the full 8 GHz clock rate output of the ALMA digitizer(s) (with samples limited to 2-bits). In this mode, each one millisecond of the full bandwidth signal at the station card input is split into 32 one millisecond packets, each with a 125 MHz clock rate, in the station card RAM buffer. The 32 packets are routed to 32 correlator planes (see below) where cross correlation occurs.

4.3 Correlator Array

The basic building block of the correlator system is a matrix of 64-by-64 correlator blocks referred to as a correlator “plane”. A correlator plane provides a 2048-lag correlator circuit at each of the intersections of the matrix (a correlator plane thus has 64x64x2048 total correlator lags). Each 2048 lag circuit is driven by signals from two antennas and can be programmed to be a single 2048-lag block, to be two 1024-lag blocks, or to be four 512-lag blocks to support the various polarization options. For 2048 lag blocks on the diagonal of the matrix, the two antennas are the same and these yield autocorrelation results.

The next building block of the correlator system is the correlator “array” which consists of 32 correlator planes. There is one correlator array in each correlator quadrant and this array can process the full 4 GHz bandwidth for all 64 antennas for 2 baseband channels.

In the widest bandwidth (digital hybrid) mode, each of the 32 filter card outputs is processed in one of the 32 correlator planes of a correlator array (each filter card output will typically be a 62.5 MHz sub-band, Nyquist sampled with a clock rate of 125 MHz). For narrower bandwidth modes, some filter card outputs are not processed and the freed-up correlator planes are used to develop additional lags from the active filter card outputs. Lag generation for these modes is done on the station card.

In time division observations, the 32 correlator planes in a quadrant process the 32 time bins developed by the station card. Thus each plane handles 1/32 of the samples taken by an antenna digitizer and the 32 planes correlating station card time packets output 125-MHz-clock lags to keep up with the 4 GHz original sample rate.

4.4 LTA subsystem, Final Adder and Data Routing Switch

The Long Term Accumulator provides buffers, or longer term integration, for correlator chip results. The new ALMA2 correlator chips have built-in integrators. The integrators can be configured to allow the number of lags to be traded for time resolution in the correlator chip. Time resolutions of 16, 8, 4, 2 and 1 msec are possible with this scheme. Data are dumped from the correlator chips to the LTA on 16-msec boundaries. The Long Term Integration functionality will be implemented on the same card that contains the correlator chips.

The LTA Adder Tree functionality shown in Fig. 1 is implemented on the Final Adder cards. There are two such cards in each quadrant. The Final Adder cards have

several purposes. First, each card adds the results of up to half the baselines for modes where multiple results must be added together. Second, the Final Adder cards provide the necessary multiplication (shifting) and addition of correlator results in planes that require this operation for support of 16 level correlation. Finally, the Final Adder cards packetize the data into 10 GbE frames (Ethernet+UDP(jumbo frame)) for transmission to the CDP cluster via a Data Routing Switch, a commercial Ethernet SFP+ Switch. This allows auto-correlations to be distributed to all CDPs by multicast. The switch also performs the functions of the original cross-bar in the Final Adder, routing required sets of correlation results to the required CDPs. A design that does not need a switch is also under consideration.

The control functionality of the original LTA will remain.

4.5 Control Cards

There are three types of control cards in the correlator system.

- Station control card (SCC)
- LTA/Correlator control card (LTA/CCC)
- Quadrant control card (QCC)

Each correlator system control card has a 16-bit Infineon C167 microprocessor that communicates with the correlator control computer over a serial CAN bus. The SCC and LTA/CCC control cards each support an 8-bit bidirectional communication bus over the bin motherboard to individual logic cards in the system. This bus is used for control and monitoring functions such as FPGA personality loading, mode programming, active observation support, and various monitoring responsibilities. The QCC monitors voltages and temperatures in the system and can force a power down when a danger is detected.

Software for the ALMA correlator control cards is written in C using a Keil software development system and version control uses CVS.

The correlator upgrade will retain the same control system. This leverages the many FTE-years of work that went into developing software and control protocols. It is expected that only minor control software changes will be required for the upgrade.

5 Performance

The performance of the ALMA correlator, in terms of bandwidth and frequency resolution, can be seen Tables 2, 3 and 4. Table 2 gives the performance of a single quadrant of the correlator in modes in which a single baseband channel of a baseband

pair is processed. Table 3 gives system performance in modes in which both baseband channels of a pair are processed but no cross correlations are performed. Table 4 gives the system performance in modes in which polarization cross correlations are generated. The achieved spectral resolution will be a factor of two poorer than the reported channel widths due to online Hanning smoothing. For additional information on achieved resolution, see

https://help.almascience.org/index.php?/Knowledgebase/Article/View/29/0/WhatspectralresolutionwillIgetforagivenchannelspacing

The sensitivity column in tables 2, 3 and 4 reflects the initial ALMA 3-bit digitizer contribution to sensitivity, assuming optimum sampler levels.

The spectral resolution of frequency division modes (FDM) scales by a factor of 8 for all modes from the original design to the upgrade design due to the additional lags present in the new correlator chip, the ALMA2. However, the spectral resolution of time division modes (TDM) does not scale this way. The spectral resolution of TDM modes is limited to 512 lags by the need to limit the loss due to “blanking time”. Further study of the loss is planned. It may be possible to increase the number of lags in TDM with minimal sacrifice in sensitivity.

6 Size and Power Requirements

Each quadrant of the correlator consists of eight digital racks, one power supply rack and one computer rack. Four of the digital racks house DRX/TFB cards, and station cards sufficient to process the output of two of the 8 baseband channels produced by 64 antennas of the ALMA array. The other 4 racks house a single correlator array and LTA/CCC cards.

Power requirements of the current correlator are about 35 kW per quadrant including the DRX/TFB cards, the CCC computer and CDP computers. Power dissipation of the upgraded correlator is expected to be less than that of the original correlator, thus the original power supply and cooling systems require no changes. The predicted amount of improvement depends greatly on the power dissipation of the new correlator ASICs which are not yet designed.

7 Phasing System Compatibility

Compatibility with the existing VLBI system shall be maintained. No changes are required for this to occur.

8 Sub-array, Multi-resolution and Phase Switching Mode Capabilities

Sub-array, multi-resolution and 90-degree phase switching mode capabilities shall be maintained. In particular, the correlator will continue to support 16 sub-arrays. Multi-resolution modes will continue to support four independent windows within given mode. ALMA Memo 556 provides more information on these modes in the context of the current correlator.

9 High Time Resolution Modes

The recent peak of interest in Fast Radio Bursts (FRBs) has prompted a request that the correlator upgrade consider adding features that would enable high time resolution observations. This feature would also be useful in other transient detection fields of astronomy such as solar.

Like the “hooks for VLBI” that were designed into the current correlator, this is a hardware-only feature that will be developed should an appropriate project be approved. The hardware includes two SFP+ connector cages on each Final Adder Card. These are connected to the same FPGAs that send lags to the CDPs. Thus the SFP+ connectors have access to the same data being sent to the CDPs. The programmability of the FPGA devices allows great flexibility in selecting the lags to be output on these ports and in the formatting of the output data stream. The date rate of the SPF+ port is limited to 10 Gbps, including formatting. The time resolution of the data that can be provided via these ports has a minimum of 1 millisecond in frequency division mode and 1/32 of a millisecond in time division mode. Binary steps in time resolution are provided, e.g., 1, 2, 4, 8, … milliseconds. The number of lags that can be transmitted is a function of many variables: the number of bits per lag, the overhead of the selected formatting scheme, the capabilities of the selected transmitter, the length and quality of the fiber connecting to the receiving electronics and the ability of the receiving computer to accept the data.

There is presently no plan to provide transceivers, cables or computers capable of processing this data. All of this detail is to be determined if and when a project to take advantage of this capability is conceived.

Table 2 Mode chart with one baseband channel per quadrant being processed

Mode #	Number of sub-channel filters	Total Bandwidth	Number of Spectral Points[4]	Channel Width	Channel Width at 230 GHz[4]	Correlation	Sample Factor	Minimum dump time[1]	Sensitivity[2]
1	32	2 GHz	65536	30.5 kHz	0.04 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
19	32	2 GHz	32768	61 kHz	0.08 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.90
38	32	2 GHz	16384	122 kHz	0.16 km/s	4-bit x 4-bit	Nyquist	128 msec	0.95
2	16	1 GHz	65536	15.3 kHz	0.02 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
20	16	1 GHz	32768	30.5 kHz	0.04 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.90
39	16	1 GHz	16384	61 kHz	0.08 km/s	4-bit x 4-bit	Nyquist	128 msec	0.95
53	16	1 GHz	8192	122 kHz	0.16 km/s	4-bit x 4-bit	Twice Nyquist	64msec	0.95
3	8	500 MHz	65536	7.6 kHz	0.01 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
21	8	500 MHz	32768	15.3 kHz	0.02 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.90
40	8	500 MHz	16384	30.5 kHz	0.04 km/s	4-bit x 4-bit	Nyquist	128 msec	0.95
54	8	500 MHz	8192	61 kHz	0.08 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.95
4	4	250 MHz	65536	3.75 kHz	0.005 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
22	4	250 MHz	32768	7.6 kHz	0.01 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.90
41	4	250 MHz	16384	15.3 kHz	0.02 km/s	4-bit x 4-bit	Nyquist	128 msec	0.95
55	4	250 MHz	8192	30.5 kHz	0.04 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.95
5	2	125 MHz	65536	1.9 kHz	0.0025 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
23	2	125 MHz	32768	3.75 kHz	0.005 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.90
42	2	125 MHz	16384	7.6 kHz	0.01 km/s	4-bit x 4-bit	Nyquist	128 msec	0.95
56	2	125 MHz	8192	15.3 kHz	0.02 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.95
6	1	62.5 MHz	65536	0.95 kHz	0.00125 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
24	1	62.5 MHz	32768	1.9 kHz	0.0025 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.90
43	1	62.5 MHz	16384	3.75 kHz	0.005 km/s	4-bit x 4-bit	Nyquist	128 msec	0.95
57	1	62.5 MHz	8192	7.5 kHz	0.01 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.95
25	1	31.25 MHz	65536	0.48 kHz	0.00062 km/s	2-bit x 2-bit	Twice Nyquist	512 msec	0.90
58	1	31.25 MHz	16384	1.9 kHz	0.0025 km/s	4-bit x 4-bit	Twice Nyquist	128 msec	0.95
68	Time Division Mode	2 GHz	512	3.9 MHz	5.1 km/s	3-bit x 3-bit	Nyquist	16 msec	0.96
71	Time Division Mode	2 GHz	512[3]	3.9 MHz	5.1 km/s	2-bit x 2-bit	Nyquist	16 msec	0.88

[1] Assuming all products, all lags, transferred from correlator to Correlator Data Processor computer (in milli-seconds).

[2] Takes into account the 0.96 sensitivity degradation imposed by the 3-bit input digitizer.

[3] 2048 points could be provided, but with an additional noise and time resolution penalties

[4] The achieved spectral resolution will be a factor of two poorer than the reported channel widths due to online Hanning smoothing.

Table 3. Mode chart with two baseband channels per quadrant processed with no pol. cross products

Mode #	Number of sub-channel filters	Total Bandwidth	Number of Spectral Points[4]	Channel Width	Channel Width at 230 GHz[4]	Correlation	Sample Factor	Minimum dump time[1]	Sensitivity[2]
7	32	2 GHz	32768	61 kHz	0.08 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
8	16	1 GHz	32768	30.5 kHz	0.04 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
26	16	1 GHz	16384	61 kHz	0.08 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.90
44	16	1 GHz	8192	122 kHz	0.16 km/s	4-bit x 4-bit	Nyquist	128 msec	0.95
9	8	500 MHz	32768	15.3 kHz	0.02 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
27	8	500 MHz	16384	30.5 kHz	0.04 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.90
45	8	500 MHz	8192	61 kHz	0.08 km/s	4-bit x 4-bit	Nyquist	128 msec	0.95
59	8	500 MHz	4096	122 kHz	0.16 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.95
10	4	250 MHz	32768	7.6 kHz	0.01 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
28	4	250 MHz	16384	15.3 kHz	0.02 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.90
46	4	250 MHz	8192	30.5 kHz	0.04 km/s	4-bit x 4-bit	Nyquist	128 msec	0.95
60	4	250 MHz	4096	61 kHz	0.08 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.95
11	2	125 MHz	32768	3.8 kHz	0.005 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
29	2	125 MHz	16384	7.6 kHz	0.01 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.90
47	2	125 MHz	8192	15.3 kHz	0.02 km/s	4-bit x 4-bit	Nyquist	128 msec	0.95
61	2	125 MHz	4096	30.5 kHz	0.04 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.95
12	1	62.5 MHz	32768	1.9 kHz	0.0025 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
30	1	62.5 MHz	16384	3.8 kHz	0.005 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.90
48	1	62.5 MHz	8192	7.6 kHz	0.01 km/s	4-bit x 4-bit	Nyquist	128 msec	0.95
62	1	62.5 MHz	4096	15.3 kHz	0.02 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.95
31	1	31.25 MHz	32768	0.95 kHz	0.0012 km/s	2-bit x 2-bit	Twice Nyquist	512 msec	0.90
63	1	31.25 MHz	8192	3.8 kHz	0.005 km/s	4-bit x 4-bit	Twice Nyquist	128 msec	0.95
69	Time Division Mode	2 GHz	512[3]	3.9 MHz	5.1 km/s	2-bit x 2-bit	Nyquist	16 msec	0.88

[1] Assuming all products, all lags, transferred from correlator to Correlator Data Processor computer (in milli-seconds).

[2] Takes into account the 0.96 sensitivity degradation imposed by the 3-bit input digitizer.

[3] 1024 points could be provided, but with an additional noise and time resolution penalties

[4] The achieved spectral resolution will be a factor of two poorer than the reported channel widths due to online Hanning smoothing.

Table 4. Mode chart with two baseband channels per quadrant processed with pol. cross products, Phase 1

Mode #	Number of sub-channel filters	Total Bandwidth	Number of Spectral Points[4]	Channel Width	Channel Width at 230 GHz[4]	Correlation	Sample Factor	Minimum dump time[1]	Sensitivity[2]
13	32	2 GHz	16384	122 kHz	0.16 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
14	16	1 GHz	16384	61 kHz	0.08 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
32	16	1 GHz	8192	122 kHz	0.16 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.90
15	8	500 MHz	16384	30.5 kHz	0.04 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
33	8	500 MHz	8192	61 kHz	0.08 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.90
16	4	250 MHz	16384	15.3 kHz	0.02 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
34	4	250 MHz	8192	30.5 kHz	0.04 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.90
17	2	125 MHz	16384	7.6 kHz	0.02 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
35	2	125 MHz	8192	15.3 kHz	0.04 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.90
51	2	125 MHz	4096	30.5 kHz	0.02 km/s	4-bit x 4-bit	Nyquist	128 msec	0.95
18	1	62.5 MHz	16384	3.8 kHz	0.005 km/s	2-bit x 2-bit	Nyquist	512 msec	0.84
36	1	62.5 MHz	8192	7.6 kHz	0.01 km/s	2-bit x 2-bit	Twice Nyquist	256 msec	0.90
52	1	62.5 MHz	4096	15.3 kHz	0.02 km/s	4-bit x 4-bit	Nyquist	128 msec	0.95
66	1	62.5 MHz	2048	30.5 kHz	0.04 km/s	4-bit x 4-bit	Twice Nyquist	64 msec	0.95
37	1	31.25 MHz	16384	1.9 kHz	0.0025 km/s	2-bit x 2-bit	Twice Nyquist	512 msec	0.90
67	1	31.25 MHz	4096	7.6 kHz	0.01 km/s	4-bit x 4-bit	Twice Nyquist	128 msec	0.95
70	Time Division Mode	2 GHz	512	3.9 MHz	5.1 km/s	2-bit x 2-bit	Nyquist	32 msec	0.88

[1] Assuming all products, all lags, transferred from correlator to Correlator Data Processor computer (in milli-seconds).

[2] Takes into account the 0.96 sensitivity degradation imposed by the 3-bit input digitizer.