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STMicroelectronics (F-Grenoble)

ALMA 3-bit, 4Gsps Analog-to-Digital Converter

Data Sheet*

***This data sheet may contain preliminary information still subject to change.**

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ALMA

3-bit, 4Gsps, 2.5V ADC

General Description

The VEGA chip is a 2.5V, 3-bit, 2-4GHz input bandwidth, 4Gsps analog-to-digital converter (ADC) featuring an input amplifier with output common mode feed back loop, an analog bandwidth of up to 4GHz, and an internal test mode to check with a low frequency internal clock that the output bits are functionally toggling. VEGA uses the BiCMOS 0.25µm SiGe technology from STMicroelectronics.
The analog input stage allows single-ended or differential signals. VEGA is optimized for low-power, high dynamic performances and temporal stability.
Powered from 2.3V to 2.7V supply, VEGA dissipates around 1.4W with a sampling frequency of 4GHz.
The design of this ADC is robust against temperature variations thus providing a high temporal stability (total power Allan variance > 100s). The VEGA chip is designed as a flash converter ADC using two external voltage references to generate its internal references. It supports single-ended 4GHz input clock. An internal encoder transforms the thermometer code from the comparators into a Gray code. The output synchronization is made by D-Latches placed ahead of the LVDS output buffers.
VEGA is available in an ESD-protected, 7mm x 7mm x 1mm, 44-pin VFQFN package.

Application

- **High Speed Data Acquisition**
- **Astronomical / Passive Observations**
- **Power Statistic Acquisition**

Features

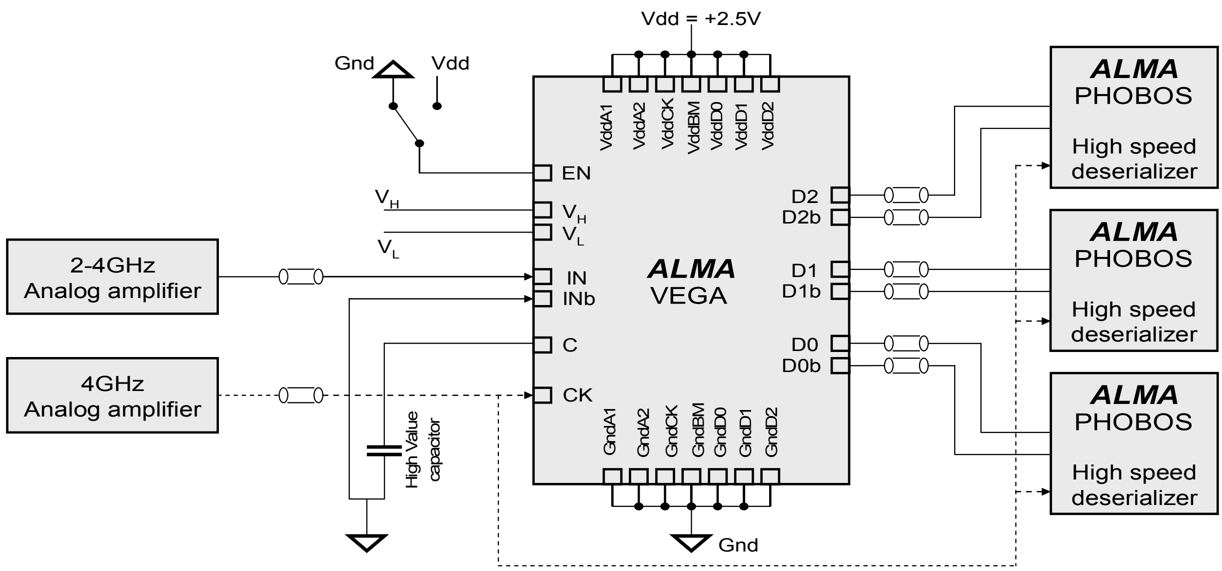
- **Single 2.5V power supply**
- **Sampling frequency 4GHz**
- **Resolution 3-Bits**
- **Input Bandwidth 2-4GHz**
- **Differential or Single-Ended Analog Input**
- **Input Peak Voltage Proof**
- **High Temporal Stability**
- **LVDS Compatible Outputs in Gray Code**
- **Test Mode Implementation**
- **44-Pin VFQFPN Package**

Ordering Information

Name	Temperature range	Pin-Package
VEGA	-20°C to +70°C	44-Pin VFQFPN (7mm x 7mm x 1mm)

Typical Operating Circuit

Fig.1: Block diagram of *ALMA* 3-bit ADC followed by 3 deserializer chips



: This symbol represents a transmission line of characteristic impedance Z0 = 50Ω

Absolute Maximum Ratings

Vdd to Gnd ....-0.3V to 2.8V
IN, INb to Gnd …………………-0.3V to Vdd + 0.3V
V_H, V_L to Gnd ....…………-0.3V to Vdd + 0.3V
C to Gnd ....-0.3V to Vdd + 0.3V
CK to Gnd....................................-0.3V to Vdd + 0.3V
D0, D0b, D1, D1b, D2, D2b ....-0.3V to Vdd + 0.3V
Operating Temperature Range ....-20°C to +70°C
Operating Relative humidity range ....20% to 80%
Storage Temperature ....-30°C to +100°C
Lead Temperature (soldering 10s) ....+250°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damages to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Expose to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical & Dynamic Characteristics

(Vdd = +2.3V to +2.7V, differential loads = 100Ω ± 1%, $T_{Ambient}$ = -20°C to +70°C, unless otherwise noted. Typical values are at Vdd = 2.5V, $T_{Ambient}$ = 25°C)

Table 1. Technical Specifications

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution					3	Bits
Indecision Level					10	mV
ANALOG INPUT (IN, INb)						
Differential Input Power	V_{DIFF}			-10	0	dBm
Common Mode Input Voltage			Gnd + 0.3		Vdd - 0.3	V
Input Impedance				50		Ω
Input Cross-talk (@4GHz)				-46	-40	dB
CONVERSION RATE						
Clock Frequency	f_{CLK}		0.5	4	5	GHz
Data Latency				1.5		Clock Cycles
DYNAMIC CHARACTERISTICS (single-ended inputs with f_{CLK} = 4GHz)						
Stability (Allan Variance)		With Vdd to Gnd = 2.5V	100			s
CLOCK INPUT (CLK)						
Common Mode Input Voltage			Gnd – 0.8	Gnd	Vdd + 0.8	V
Input Power			-10	0	5	dBm
Input Impedance				50		Ω
DIGITAL OUTPUTS (D0, D0b, D1, D1b, D2, D2b)						
Differential Output Impedance			80	100	120	Ω
Common Mode Voltage Signal			0.925		1.475	V
Differential Voltage			250		400	mV
POWER REQUIREMENTS						
Analog Supply Voltage	VddA1, VddA2		2.4	2.5	2.6	V
Digital Supply Voltage	VddCK,VddBM		2.3	2.5	2.7	V
LVDS Output Buffer Supply Voltage	VddD0, VddD1, VddD2		2.3	2.5	2.7	V
Analog supply Current	IddA1		103		149	mA
	IddA2		95		142	mA
Digital Supply Current	IddCK		81		119	mA
	IddBM	With Vdd to Gnd = 2.5V	137		172	mA
LVDS Output Buffer Supply Current	IddD0		24		39	mA
	IddD1		24		39	mA
	IddD2		24		39	mA
TIMING CHARACTERISTICS						
Data-Valid Delay	t_{DAV}		85		130	ps
Data Rising Edge Time					80	ps
Data Falling Edge Time					80	ps
Data synchronization error					50	ps

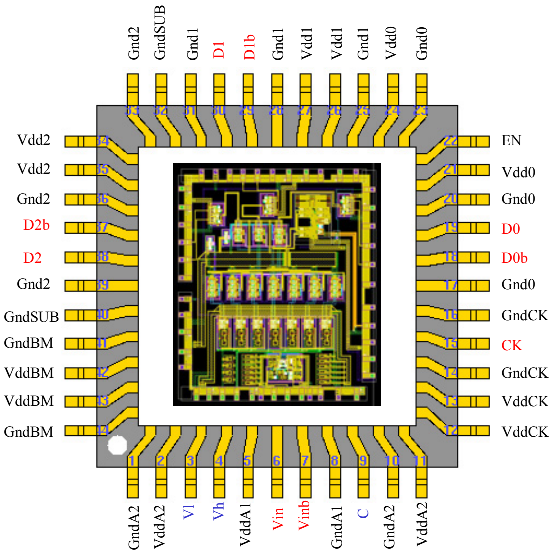


Fig.2: ***ALMA*** **chip photograph and pin-out**

Transistors count: 720

Table 2. Pin-out description

NAME	PIN	DESCRIPTION
VddA1	5	Positive Supply Voltage for the Analog Input Amplifier
GndA1	8	Negative Supply Voltage for the Analog Input Amplifier
VddA2	2, 11	Positive Supply Voltage for the Comparators
GndA2	1, 10	Negative Supply Voltage for the Comparators
VddCK	12, 13	Positive Supply Voltage for the Clock amplifier
GndCK	14, 16	Negative Supply Voltage for the Clock amplifier
VddBM	42, 43	Positive Supply Voltage for the Digital Part
GndBM	41, 44	Negative Supply Voltage for the Digital Part
VddD0	21, 24	Positive Supply Voltage for the LVDS Output Buffer of D0
GndD0	17, 20, 23	Negative Supply Voltage for the LVDS Output Buffer of D0b
VddD1	26, 27	Positive Supply Voltage for the LVDS Output Buffer of D1
GndD1	25, 28, 31	Negative Supply Voltage for the LVDS Output Buffer of D1b
VddD2	34, 35	Positive Supply Voltage for the LVDS Output Buffer of D2
GndD2	33, 36, 39	Negative Supply Voltage for the LVDS Output Buffer of D2b
GndSUB	32, 40	Substrate Contact
C	9	Low-Pass Filter Capacitor
Vin	6	Analog Input
Vinb	7	Complement Analog Input
Vl	3	High Reference Voltage
Vh	4	Low Reference Voltage
CK	15	Clock
D0	19	LVDS Output Data D0
D0b	18	LVDS Output Data D0b
D1	30	LVDS Output Data D1
D1b	29	LVDS Output Data D1b
D2	38	LVDS Output Data D2
D2b	37	LVDS Output Data D2b
EN	22	Test Enable

Detailed Typical Operating Circuit

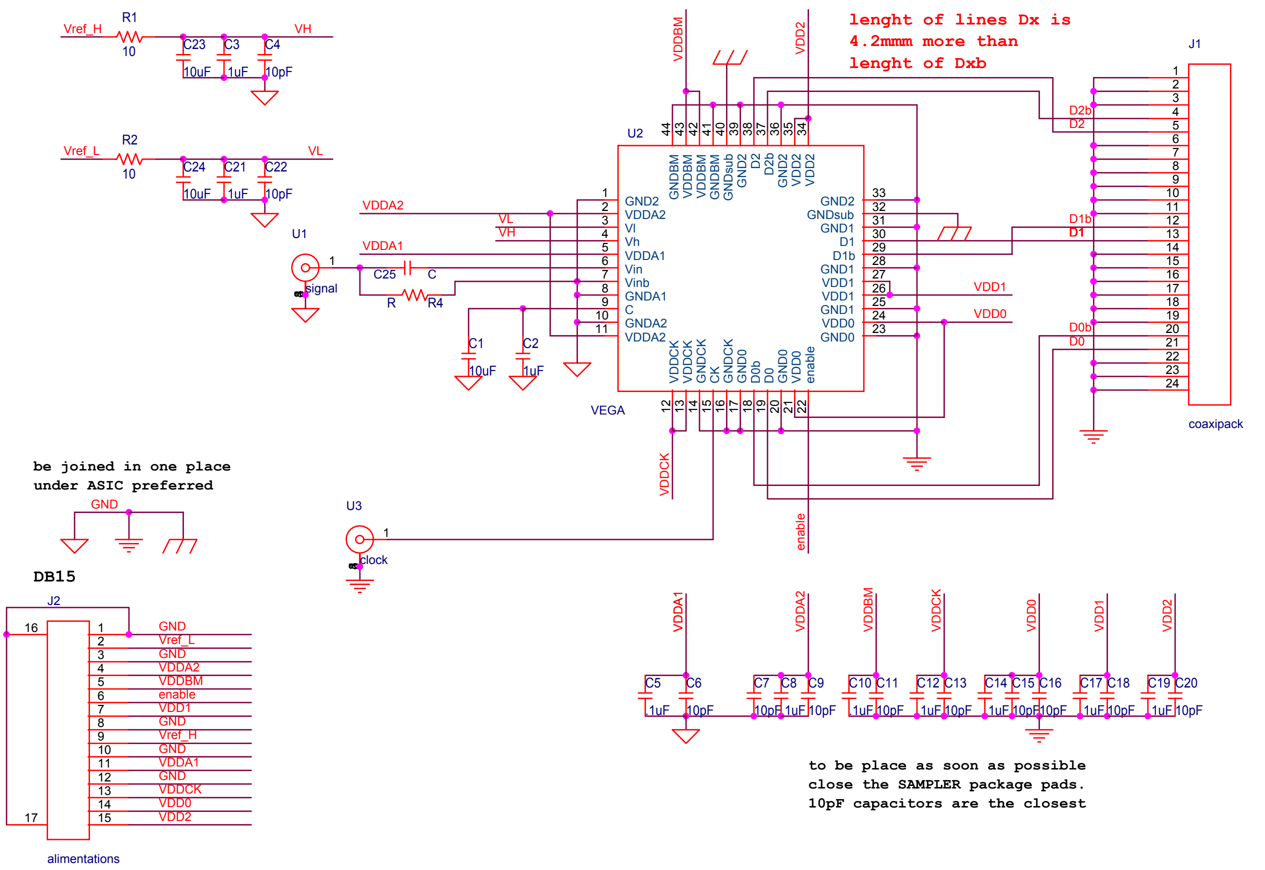


Fig. 3: Example of operating circuit

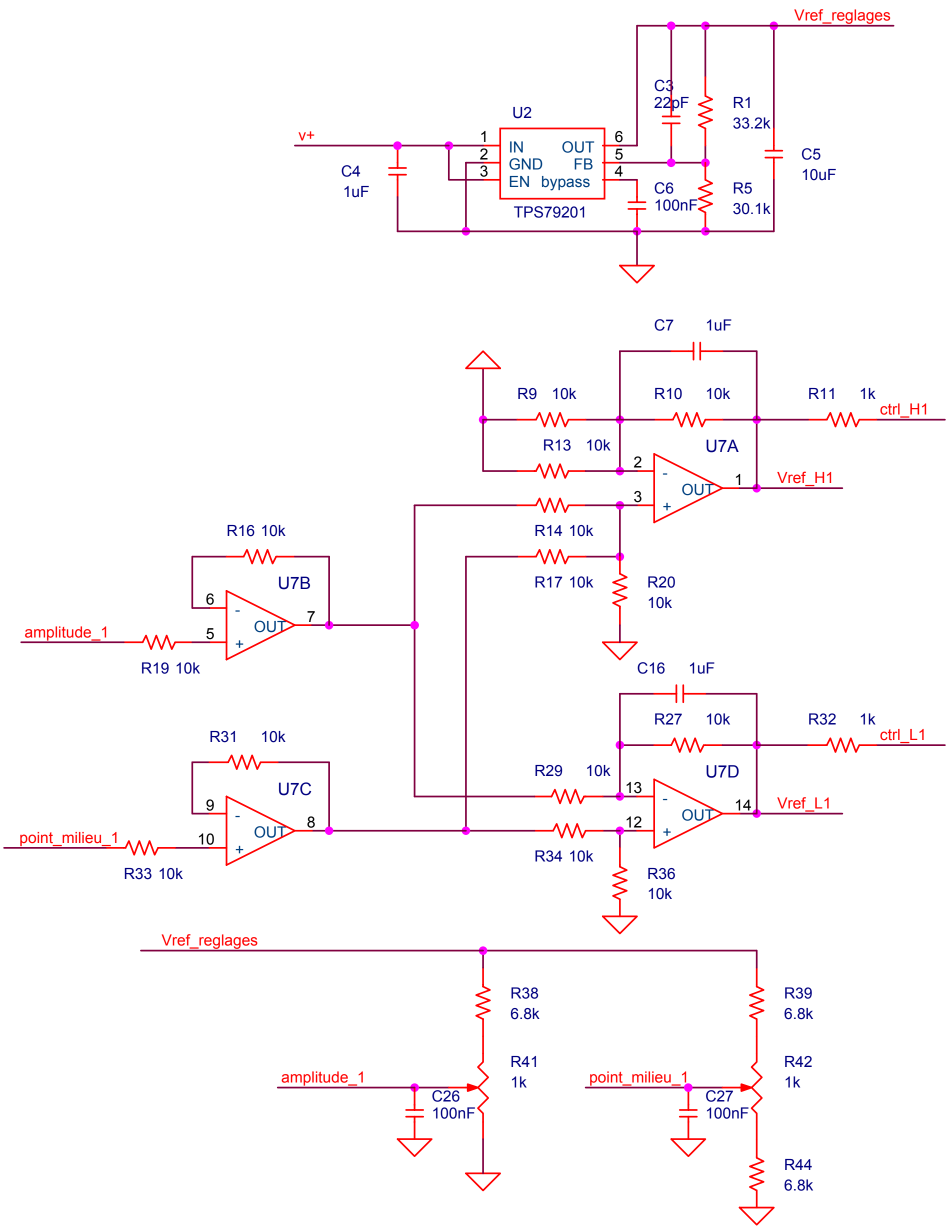


Fig. 4: Example of voltage reference generator circuit

3-bit, 4Gsps, 2.5V ADC

Flash ADC Architecture

The ADC integrates an input adapter amplifier, seven comparators (one per comparison level) with associated latches, an encoder matrix and three output buffers.

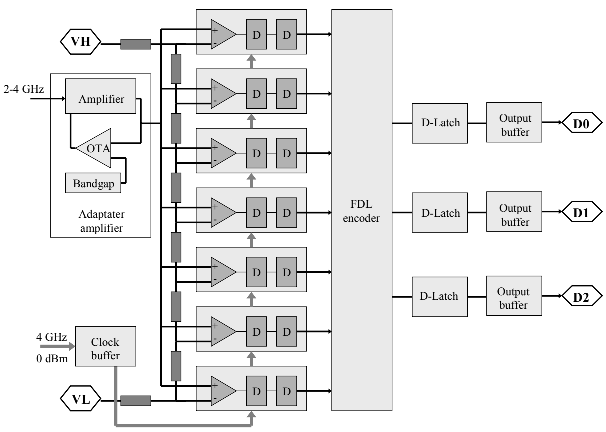


Fig. 5: Functional Diagram

The 2GHz bandwidth input signal is amplified and compared with the different thresholds before encoding. The output buffers deliver LVDS signals.

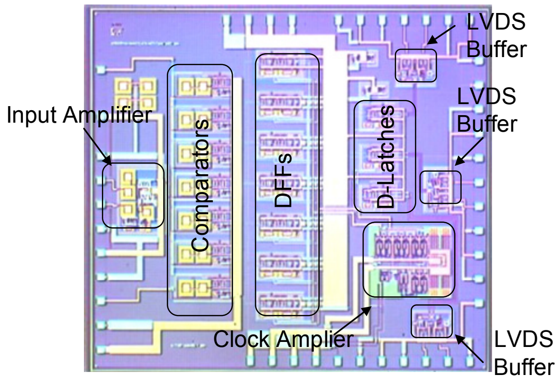


Fig. 6: ADC chip architecture

Input Amplifier

The input adapter amplifier is an analog stage performing 50Ω input matching across the overall band. It amplifies and converts the input signal into a differential one before the sampling cells.
The input bandwidth goes up to 4GHz. The response of this amplifier is linear and the ripple over the band is less than 0.5dB according to simulations.

A common mode feedback loop is implemented to stabilize the mean voltage at the amplifier output in spite of temperature and process variations. The output common mode voltage is compared with a voltage reference generated by a bandgap cell. The OTA output is filtered with a low pass filter, and this voltage drives the current generator of the differential pair.

Comparators

The comparators consist of two amplification stages. This structure suppresses the metastability states by providing more amplification of the input signal which decreases the indecision level and thus provides better conversion speed by holding the state comparison result.

Sampler

A DFF latch placed after the comparators, in a master-slave configuration, performs the sampling function by memorizing the comparator outputs. This DFF consists of two D-latches driven in opposition by the same clock.

Clock Amplifier

A dedicated clock amplifier is integrated to drive the pseudo-differential latches. The first levels of this stage use voltage amplifiers while the last ones are current amplifiers in order to increase the fan-out needed by the great number of latches. A dedicated current amplifier is designed to cancel the static current and decrease the power consumption.

Encoder

The folding differential logic (FDL) encoder converts the comparators results into a Gray code. The encoding process is realized using current mode technique thanks to the association of several current generators.

Gray Code Description

Voltage	Code (D2 / D1 / D0)
Vref7 < V	1 / 0 / 0
Vref6 < V < Vref7	1 / 0 / 1
Vref5 < V < Vref6	1 / 1 / 1
Vref4 < V < Vref5	1 / 1 / 0
Vref3 < V < Vref4	0 / 1 / 0
Vref2 < V < Vref3	0 / 1 / 1
Vref1 < V < Vref2	0 / 0 / 1
V < Vref1	0 / 0 / 0

Table 3. ***ALMA*** **sampler Gray code**

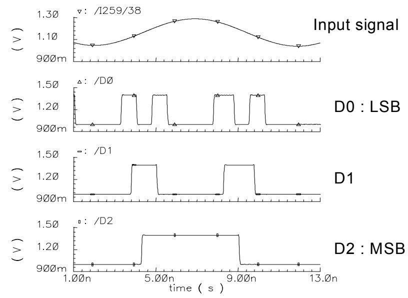


Fig. 7: D2 (sign), D1, D0 bit encoding

LVDS Output Buffers

The output buffers are implemented to convert the encoder outputs into a signal compatible with the LVDS standard. The output voltage swing is fixed by two resistors in the differential pair and the current source.
An R-C filter has been integrated before the output PADs in order to decrease the transition time and the parasitic effects due to the chip bonding.

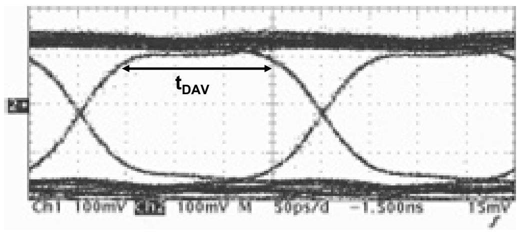


Fig. 8: Output eye diagram

Test Mode Description

In order to validate with standard low frequency equipment the functionality of the VEGA sampler after it has been manufactured and packaged, a test clock generator has been implemented within the chip. The goal of this cell is to check the functionality of the circuit but not its performances. Thus, it is not mandatory to operate at 4GHz and to use a clock with good spectral purity.

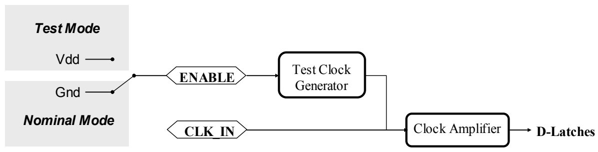


Fig. 9: Localization of the test clock generator

The clock generator works around 800MHz.

Threshold Spacing

The 7-threshold comparators of the ALMA digitizer are equally distributed over the input dynamic range so that the data amplitude histogram produces a Gaussian probability distribution function.

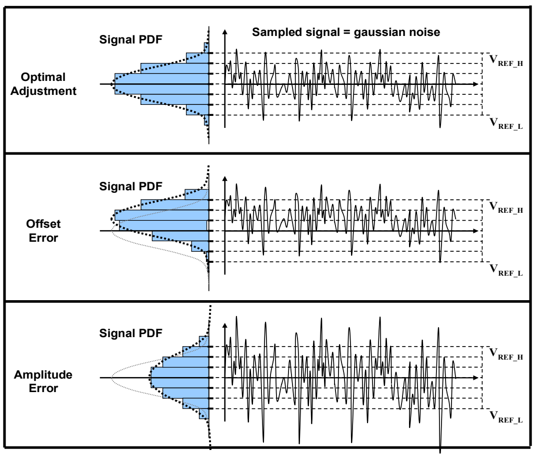


Fig. 10: Distortion of probability distribution function

Measurement of the sampled data statistical distribution points out any static offset due to incorrect position of the voltage thresholds or any dynamic offset due to input overdriving or clock feedback on the analog input.

Thanks to the common mode feedback loop, the statistic distribution does not shift with temperature variations. When this loop is disabled, the distribution changes with the temperature thus demonstrating the temperature immunity of the ALMA converter.

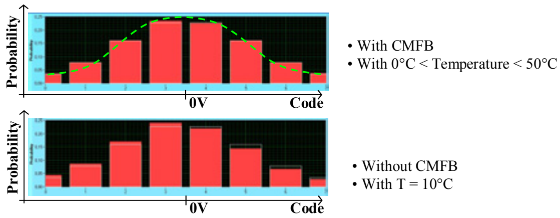


Fig. 11: Statistic distribution with and without the common mode feed back loop (CMFB).

3-bit, 4Gsps, 2.5V ADC

Converter Frequency Response

In order to achieve a flat spectral response on application PCBs across 2-4GHz bandwidth, a passive high pass filter may be implemented outside the chip on the PCB to compensate for transfer losses in the PCB and connectors and to correct parasitic effects due to metallic lines within the chip

For ALMA applications less than ± 0.5dB ripple is achieved with two selected passive components assembled on the PCB.

Converter Stability

Time stability of an ADC over long integration periods as is often required in radioastronomy or in passive observations is estimated according to the Allan variance (or two-sample variance) of the sampled data. The accuracy of this statistical estimator increases with the number of analyzed samples provided that one uses stationary data.

The Allan variance is estimated by splitting the data set into N slices of τ duration. For each time segment one derives the mean value and the variance of this statistical value over the whole set of time slices; the same derivation is then performed with an increased τ duration.

For the ALMA ADC, Allan variance measurements are performed up to 100s or above using the zeroth lag (equivalent to digitized total power) from a dedicated autocorrelator system.

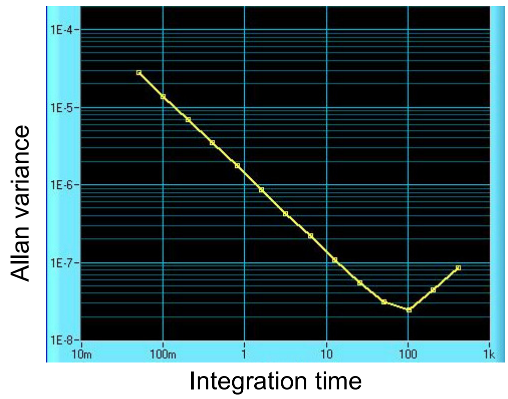


Fig. 12: Typical Allan variance of ALMA digitizer

Data Latency

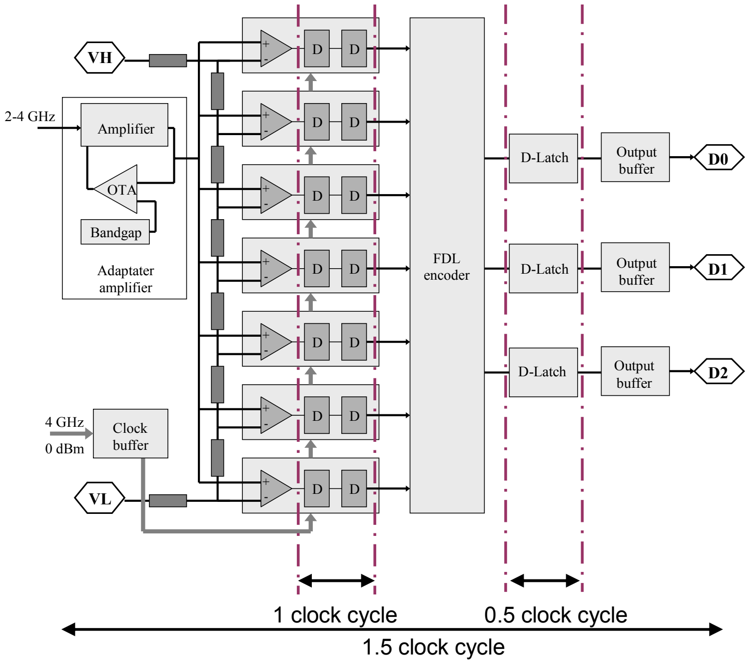


Fig. 13: Data latency localization.

Package Name: VFQFPN 7x7x1.0 44L PITCH 0.50

	DIMENSIONS					
	DATABOOK (mm)			DRAWING (mm)		
REF.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.800	0.900	1.000	0.800	0.850	1.000
A1		0.020	0.050		0.010	0.050
A2		0.650	1.000		0.650	0.800
A3		0.250			0.200	
b	0.180	0.230	0.300	0.204	0.254	0.300
D	6.875	7.000	7.125	6.900	7.000	7.100
D2	2.250	4.700	5.250	SEE EXPOSED PAD VARIATIONS		
E	6.875	7.000	7.125	6.900	7.000	7.100
E2	2.250	4.700	5.250	SEE EXPOSED PAD VARIATIONS		
e	0.450	0.500	0.550	0.450	0.500	0.550
L	0.350	0.550	0.750	0.500	0.600	0.750
ddd			0.080			0.050

	EXPOSED PAD VARIATIONS					
	D2			E2		
VARIATION	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.550	4.700	4.850	4.550	4.700	4.850
B	3.150	3.300	3.450	3.150	3.300	3.450
C	3.650	3.800	3.950	3.650	3.800	3.950

NOTES:

(1) -VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Package No lead.
- Very thin: A = 1.00 Max.

(2) – Details of terminal 1 identifier are optional but must be located on the top surface of the package by using either a mold or marked features.