Monitor and Control Firmware

KFPA Critical Design Review

Overview

- General requirements
- Single pixel approach
- Multiple pixel approach

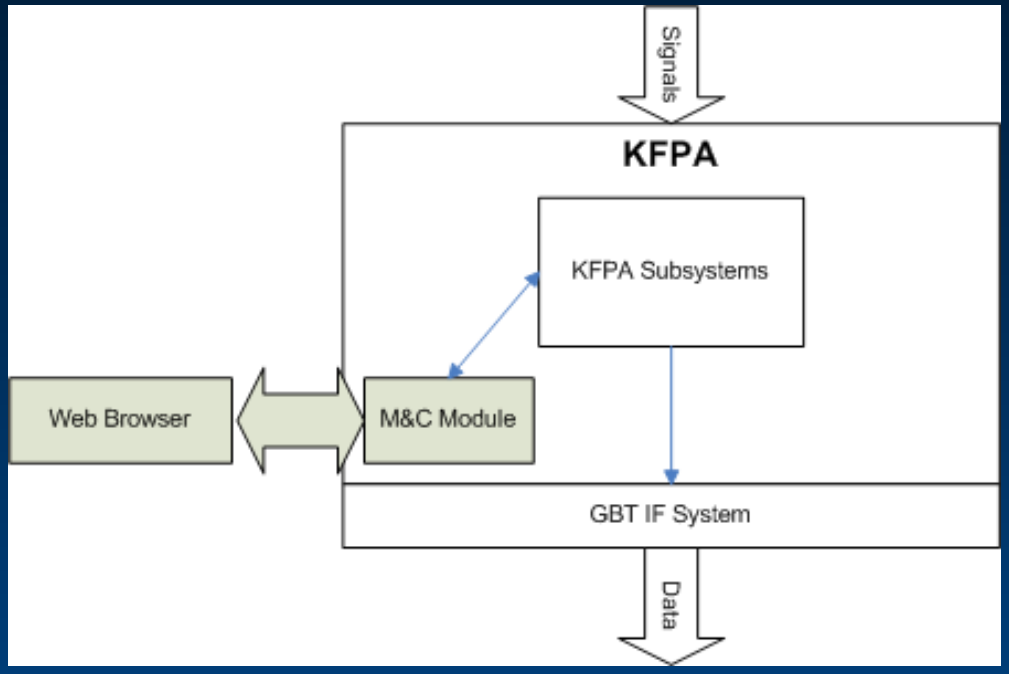
General Requirements

- **GBT Network Interface Standard:** 10/100 Ethernet
- **Sub-Module Interface Standard:** Inter-Integrated Circuit serial bus with additional sub-module enable function
- **Bus Clock Frequency:** Initially 200K Hz with potential to increase to 400K Hz
- **Subsystem Segregation:** Multiple serial buses from microcontroller, each subsystem on a unique bus
- **Sub-module Selection:** Via I/O expanders on IIC bus and control lines from microcontroller
- **RFI Mitigation:** During observing scans bus activity and clocks can be suspended

(from KFPA Receiver Monitor and Control System Specification)

Single Pixel

- Commercial, off-the-shelf microcontroller
- Web page based user interface
- Generated-HTML data display
- Hardware interface through Inter-Integrated Circuit (IIC)

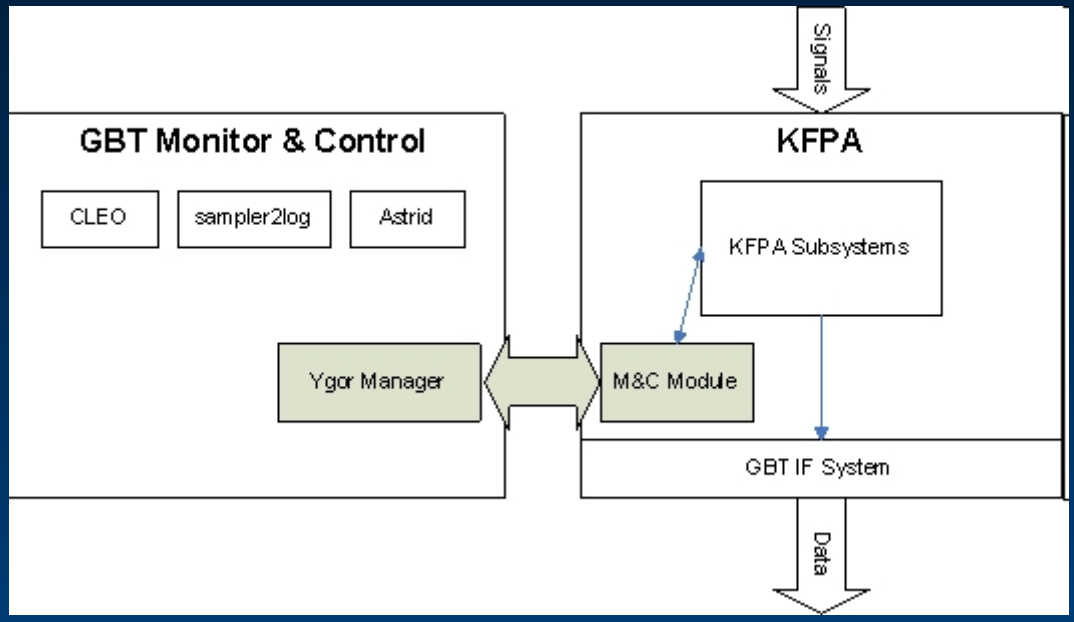


Single Pixel Results

- The speed of the IIC bus exceeded expectations
  - Able to run above 400K Hz, only required to run at 200K Hz
- HTTP works passably well for a single pixel
  - But restrictive in what forms of data and commands can be sent
  - A more flexible approach to managing pixels and transmitting data is needed for expansion

Multi-Pixel

- Changes
  - Communication to manager via TCP/IP
  - Information/commands passed via custom protocol
- Still uses IIC as the hardware interfacing method



Future Roadmap

- Determine how much “intelligence” can feasibly reside on chip
- Design specifics
  - Addressing
  - Manager-firmware communication protocol