# Updated Instances and Instance-Names for the VPM Manager

This document lists out the instance names to be used in the future release of VPM firmware models. The changes have been proposed and presented, primarily to:

(i) Avoid naming discrepancies between newer-version builds, and the manager.
(ii) Update the VPM Manager with the details of the new blocks added.
(iii) Maintain a similar convention for VPM and Spectral-line managers, for a smoother/easier integration of the two, in the future. This is done by using an 'all-lower-case' naming, as currently used in the spectral-line firmware and manager.

In order to assist the SW division to update the manager, with the necessary changes, a brief summary of the changes incorporated to the latest VPM firmware are as follows,

**New blocks added to the VPM firmware to both INCO and CoDD modes:**

1. ***adcsnap0/adcsnap1***: These blocks (including 'trigger' register) have been added, and they retain the same naming convention as in the Spectral-line manager. The instances therefore to be added to the VPM managers are:

trig
adcsnap0_bram
adcsnap0_ctrl
adcsnap0_status
adcsnap1_bram
adcsnap1_ctrl
adcsnap1_status

2. ***Switching Signal block***: This block (including 'n_chan' and 'timesel' register) also retains the same instance naming convention as in the Spectral-line manager. Therefore, the corresponding instance names for this addition would be:

timesel
n_chan
ssg_gpio_in
ssg_gpio_out
ssg_length
ssg_lut_bram
ssg_ms_sel
ssg_status_out

3. ***Design ID***: This SW register has been added to provide a brief detail of the bandwidth, channels and the build-date of the design under test. The ID is in a 'BWCHMMDDYY' format, where BW is represented in multiples of 100 MHz, CH is in represented in the power-raised-to-2, and MMDDYY correspond to month, date and year of build. As an example, An 800 MHz design, with 512 channels, built on March 7, 2015 will have the ID that would look like '0809030715'.

design_id

4. ***Platform of build***: This SW register has been added to carry the Xilinx version, and the build version of a design on a given day, in a 'XILB' format, where XIL is the three digit Xilinx version (without the

decimal point), and B is the build version. So the 3rd version of a certain build on Xilinx 14.6 would look like '1463'.

plat_bd

**Current VPM blocks with updated names:**

1. ***Accumulator length***: This SW register name (INCO mode) has been changed, to maintain consistency between the VPM and Spectral-line managers

ACC_LENGTH → acc_len

2. ***FFT Shift:*** This SW register name (INCO and CoDD) has been changed, to maintain consistency between the VPM and Spectral-line managers

FFT_SHIFT → fftshift

3. ***Ten GbE blocks:*** These 10GbE block names (INCO and CoDD) has been changed, to maintain consistency between the VPM and Spectral-line managers

INCO modes: tGv20 → gbe0

CODD modes:
tGX8_tGv20 → gbe0
tGX8_tGv21 → gbe1
tGX8_tGv22 → gbe2
tGX8_tGv23 → gbe3
tGX8_tGv24 → gbe4
tGX8_tGv25 → gbe5
tGX8_tGv26 → gbe6
tGX8_tGv27 → gbe7

4. ***10GbE overflow status:*** This SW register name (INCO and CoDD) has been changed, to maintain consistency between the VPM and Spectral-line managers.

Note: 1. In CoDD designs, this single register provides us with a composite signal, formed by 'logical OR' operation on all of the eight 10GbE modules.
2. The composite signal 'status' register, currently used in the spectral line manager to be discontinued in future builds, and will be replaced with this register.

VPM Manager: TXOF_STATUS → gbe_overflow

5. ***10 GbE Reset***: This SW register name (INCO and CoDD) has been changed, to maintain consistency between the VPM and Spectral-line managers

tenGB_reset → reset

**Blocks to be updated to lower-case:**

In the final case, the following blocks retain their existing names, however all the upper-case block names have been re-assigned with the same lower-case names. The manager therefore, needs to be updated accordingly. This was again done in order to maintain consistency among the two managers.

***INCO-modes:***

| Current VPM Manager Instance names | Updated Firmware Instance names |
|---|---|
| ARM | arm |
| DC_EN | **DISCONTINUED IN FUTURE BUILDS** |
| DEST_IP | dest_ip |
| DEST_PORT | dest_port |
| I_Vacc_I_EVEN_BRAM | i_vacc_i_even_bram |
| I_Vacc_I_ODD_BRAM | i_vacc_i_odd_bram |
| OFFSET_I | offset_i |
| OFFSET_Q | offset_q |
| OFFSET_U | offset_u |
| OFFSET_V | offset_v |
| P0_DC_SAMP_0_BRAM | **DISCONTINUED IN FUTURE BUILDS** |
| P0_DC_SAMP_1_BRAM | **DISCONTINUED IN FUTURE BUILDS** |
| P0_DC_SAMP_2_BRAM | **DISCONTINUED IN FUTURE BUILDS** |
| P0_DC_SAMP_3_BRAM | **DISCONTINUED IN FUTURE BUILDS** |
| P1_DC_SAMP_0_BRAM | **DISCONTINUED IN FUTURE BUILDS** |
| P1_DC_SAMP_1_BRAM | **DISCONTINUED IN FUTURE BUILDS** |
| P1_DC_SAMP_2_BRAM | **DISCONTINUED IN FUTURE BUILDS** |
| P1_DC_SAMP_3_BRAM | **DISCONTINUED IN FUTURE BUILDS** |
| Q_Vacc_Q_EVEN_BRAM | q_vacc_q_even_bram |
| Q_Vacc_Q_ODD_BRAM | q_vacc_q_odd_bram |
| raw_adc_trig | **DISCONTINUED IN FUTURE BUILDS** |
| SCALE_I | scale_i |
| SCALE_Q | scale_q |
| SCALE_U | scale_u |
| SCALE_V | scale_v |
| U_Vacc_U_EVEN_BRAM | u_vacc_u_even_bram |
| U_Vacc_U_ODD_BRAM | u_vacc_u_odd_bram |
| V_Vacc_V_EVEN_BRAM | v_vacc_v_even_bram |
| V_Vacc_V_ODD_BRAM | v_vacc_v_odd_bram |

***CoDD-modes:***

| Current VPM Manager Instance names | Updated Firmware Instance names |
|---|---|
| ARM | arm |
| DC_EN | **DISCONTINUED IN FUTURE BUILDS** |
| IP_0 | ip_0 |
| IP_1 | ip_1 |
| IP_2 | ip_2 |
| IP_3 | ip_3 |
| IP_4 | ip_4 |
| IP_5 | ip_5 |
| IP_6 | ip_6 |
| IP_7 | ip_7 |
| MB_MB_0_B0H | ds_to_tgbe_mb_mb_0_b0h |
| MB_MB_0_B0L | ds_to_tgbe_mb_mb_0_b0l |
| MB_MB_0_B1H | ds_to_tgbe_mb_mb_0_b1h |
| MB_MB_0_B1L | ds_to_tgbe_mb_mb_0_b1l |
| MB_MB_0_B2H | ds_to_tgbe_mb_mb_0_b2h |
| MB_MB_0_B2L | ds_to_tgbe_mb_mb_0_b2l |
| MB_MB_0_B3H | ds_to_tgbe_mb_mb_0_b3h |
| MB_MB_0_B3L | ds_to_tgbe_mb_mb_0_b3l |
| MB_MB_1_B0H | ds_to_tgbe_mb_mb_1_b0h |
| MB_MB_1_B0L | ds_to_tgbe_mb_mb_1_b0l |
| MB_MB_1_B1H | ds_to_tgbe_mb_mb_1_b1h |
| MB_MB_1_B1L | ds_to_tgbe_mb_mb_1_b1l |
| MB_MB_1_B2H | ds_to_tgbe_mb_mb_1_b2h |
| MB_MB_1_B2L | ds_to_tgbe_mb_mb_1_b2l |
| MB_MB_1_B3H | ds_to_tgbe_mb_mb_1_b3h |
| MB_MB_1_B3L | ds_to_tgbe_mb_mb_1_b3l |
| MB_MB_2_B0H | ds_to_tgbe_mb_mb_2_b0h |
| MB_MB_2_B0L | ds_to_tgbe_mb_mb_2_b0l |
| MB_MB_2_B1H | ds_to_tgbe_mb_mb_2_b1h |
| MB_MB_2_B1L | ds_to_tgbe_mb_mb_2_b1l |
| MB_MB_2_B2H | ds_to_tgbe_mb_mb_2_b2h |
| MB_MB_2_B2L | ds_to_tgbe_mb_mb_2_b2l |
| MB_MB_2_B3H | ds_to_tgbe_mb_mb_2_b3h |
| MB_MB_2_B3L | ds_to_tgbe_mb_mb_2_b3l |
| MB_MB_3_B0H | ds_to_tgbe_mb_mb_3_b0h |
| MB_MB_3_B0L | ds_to_tgbe_mb_mb_3_b0l |
| MB_MB_3_B1H | ds_to_tgbe_mb_mb_3_b1h |

| | |
|---|---|
| MB_MB_3_B1L | ds_to_tgbe_mb_mb_3_b1l |
| MB_MB_3_B2H | ds_to_tgbe_mb_mb_3_b2h |
| MB_MB_3_B2L | ds_to_tgbe_mb_mb_3_b2l |
| MB_MB_3_B3H | ds_to_tgbe_mb_mb_3_b3h |
| MB_MB_3_B3L | ds_to_tgbe_mb_mb_3_b3l |
| MB_MB_4_B0H | ds_to_tgbe_mb_mb_4_b0h |
| MB_MB_4_B0L | ds_to_tgbe_mb_mb_4_b0l |
| MB_MB_4_B1H | ds_to_tgbe_mb_mb_4_b1h |
| MB_MB_4_B1L | ds_to_tgbe_mb_mb_4_b1l |
| MB_MB_4_B2H | ds_to_tgbe_mb_mb_4_b2h |
| MB_MB_4_B2L | ds_to_tgbe_mb_mb_4_b2l |
| MB_MB_4_B3H | ds_to_tgbe_mb_mb_4_b3h |
| MB_MB_4_B3L | ds_to_tgbe_mb_mb_4_b3l |
| MB_MB_5_B0H | ds_to_tgbe_mb_mb_5_b0h |
| MB_MB_5_B0L | ds_to_tgbe_mb_mb_5_b0l |
| MB_MB_5_B1H | ds_to_tgbe_mb_mb_5_b1h |
| MB_MB_5_B1L | ds_to_tgbe_mb_mb_5_b1l |
| MB_MB_5_B2H | ds_to_tgbe_mb_mb_5_b2h |
| MB_MB_5_B2L | ds_to_tgbe_mb_mb_5_b2l |
| MB_MB_5_B3H | ds_to_tgbe_mb_mb_5_b3h |
| MB_MB_5_B3L | ds_to_tgbe_mb_mb_5_b3l |
| MB_MB_6_B0H | ds_to_tgbe_mb_mb_6_b0h |
| MB_MB_6_B0L | ds_to_tgbe_mb_mb_6_b0l |
| MB_MB_6_B1H | ds_to_tgbe_mb_mb_6_b1h |
| MB_MB_6_B1L | ds_to_tgbe_mb_mb_6_b1l |
| MB_MB_6_B2H | ds_to_tgbe_mb_mb_6_b2h |
| MB_MB_6_B2L | ds_to_tgbe_mb_mb_6_b2l |
| MB_MB_6_B3H | ds_to_tgbe_mb_mb_6_b3h |
| MB_MB_6_B3L | ds_to_tgbe_mb_mb_6_b3l |
| MB_MB_7_B0H | ds_to_tgbe_mb_mb_7_b0h |
| MB_MB_7_B0L | ds_to_tgbe_mb_mb_7_b0l |
| MB_MB_7_B1H | ds_to_tgbe_mb_mb_7_b1h |
| MB_MB_7_B1L | ds_to_tgbe_mb_mb_7_b1l |
| MB_MB_7_B2H | ds_to_tgbe_mb_mb_7_b2h |
| MB_MB_7_B2L | ds_to_tgbe_mb_mb_7_b2l |
| MB_MB_7_B3H | ds_to_tgbe_mb_mb_7_b3h |
| MB_MB_7_B3L | ds_to_tgbe_mb_mb_7_b3l |
| N_CHAN | n_chan |
| P0_DC_SAMP_0_Shared_BRAM | **DISCONTINUED IN FUTURE BUILDS** |
| P0_DC_SAMP_1_Shared_BRAM | **DISCONTINUED IN FUTURE BUILDS** |
| P0_DC_SAMP_2_Shared_BRAM | **DISCONTINUED IN FUTURE BUILDS** |

| | |
|---|---|
| P0_DC_SAMP_3_Shared_BRAM | **DISCONTINUED IN FUTURE BUILDS** |
| P1_DC_SAMP_0_Shared_BRAM | **DISCONTINUED IN FUTURE BUILDS** |
| P1_DC_SAMP_1_Shared_BRAM | **DISCONTINUED IN FUTURE BUILDS** |
| P1_DC_SAMP_2_Shared_BRAM | **DISCONTINUED IN FUTURE BUILDS** |
| P1_DC_SAMP_3_Shared_BRAM | **DISCONTINUED IN FUTURE BUILDS** |
| PT_0 | pt_0 |
| PT_1 | pt_1 |
| PT_2 | pt_2 |
| PT_3 | pt_3 |
| PT_4 | pt_4 |
| PT_5 | pt_5 |
| PT_6 | pt_6 |
| PT_7 | pt_7 |
| raw_adc_trig | **DISCONTINUED IN FUTURE BUILDS** |
| SCALE_P0 | scale_p0 |
| SCALE_P1 | scale_p1 |