

Design Report

# **VEGAS Design Report**

VEGAS-001-A-REP

Version: A Status: Released

| Prepared By:             |              |            |
|--------------------------|--------------|------------|
| Name(s) and Signature(s) | Organization | Date       |
| J.Ray                    | NRAO-GB      | 2013-02-26 |
|                          |              |            |
|                          |              |            |
|                          |              |            |
|                          |              |            |
|                          |              |            |
|                          |              |            |



Design Report

Doc #:VEGAS-001-A-REPDate:2013-02-26Status:ReleasedPage:Page 2 of 31

# Change Record

| Version | Date       | Affected<br>Section(s) | Change Request # | Reason/Initiation/Remarks |
|---------|------------|------------------------|------------------|---------------------------|
| A       | 2013-02-26 | All                    | _                | First release.            |
|         |            |                        |                  |                           |
|         |            |                        |                  |                           |
|         |            |                        |                  |                           |





**Design Report** 

## **Table of Contents**

| 1 INTRODUCTION AND SCOPE  | 5  |
|---|----|
| 1.1 Scope   | 5  |
| 1.2 Introduction  | 5  |
| 1.3 Abbreviations and Acronyms  | 5  |
| 2 DOCUMENTATION   | 6  |
| 2.1 Applicable documents  | 6  |
| 2.2 Reference Documents   |    |
| 3 VEGAS ELECTRONICS DESIGN  |    |
| 3.1 Roach2 Board  |    |
| 3.1.1 Uboot Configuration   |    |
| 3.1.2 I2C Communications  |    |
| RS232 Communications  |    |
| 3.1.3 Front Panel I/O   |    |
| 3.1.4 Switching Signal Cabling  |    |
| 3.1.5 Network Connection  |    |
| 3.1.6 Power Supply  |    |
| 3.2 ASIAA 5GSPS ADC Board   |    |
| 3.2.1 ADC clock   |    |
| 3.2.2 1PPS  |    |
| 3.2.3 IF input  |    |
| 3.3 SFP+ Mezzanine Board  |    |
| 3.4 Valon Synthesizer   |    |
| 3.5 Analog IF Interface   |    |
| 3.6 Switching Signal Distribution System  |    |
| 3.7 RAL 1PPS Distributor  |    |
| 3.8 10MHz Distribution  |    |
| 4 VEGAS MECHANICAL DESIGN   |    |
| 4.1 Shielded Rack Top Plate   |    |
| 4.2 Shielded Rack Power Entry   |    |
| 4.3 Roach2 Mounting Plate   |    |
| 4.4 Roach2 Chassis  |    |
| <ul> <li>4.5 IF Module Chassis</li></ul>  |    |
|   | 23 |
| 4.7 Roach2 Power Supply Chassis   |    |
| <ul> <li>5 THERMAL ANALYSIS</li> <li>5.1 Shielded Rack Heat Calculations</li> </ul> |    |
|   |    |
|   |    |
| 6 RFI/EMI CONSIDERATIONS<br>6.1 Shielded Rack                                       |    |
|   |    |
| <ul><li>6.1.1 AC Power Entry</li><li>6.1.2 Rack Top Plate</li></ul>                 |    |
| 6.2 Valon Synthesizer   |    |
| 7 EARLY ASTRONOMICAL TESTING  |    |
|   |    |

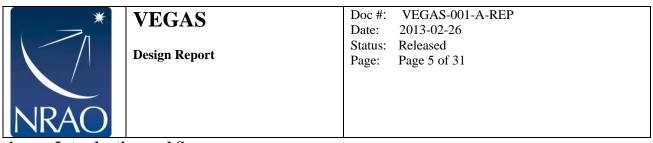


Design Report

Doc #:VEGAS-001-A-REPDate:2013-02-26Status:ReleasedPage:Page 4 of 31

### TABLE OF FIGURES

| FIGURE 1 - ROACH2 BLOCK DIAGRAM                             |
|---|
| FIGURE 2 - ROACH2 I2C BUS DETECT TEST                       |
| FIGURE 3 - VEGAS I2C CABLING 10                             |
| FIGURE 4 - PYTHON INTERFACE FOR VALON SYNTHESIZER           |
| FIGURE 5 - VEGAS RS232 CABLING 12                           |
| FIGURE 6 - VEGAS FRONT PANEL I/O CABLING                    |
| FIGURE 7 - SWITCHING SIGNAL CABLING, BRACKET 1 TO SSDS 14   |
| FIGURE 8 - SWITCHING SIGNAL CABLING, BRACKET 1 TO ROACH2 15 |
| FIGURE 9 - SWITCHING SIGNAL CABLING DETAILS 16              |
| FIGURE 10 - ROACH2 POWER SUPPLY WIRING 17                   |
| FIGURE 11 - 5GSPS ADC BOARD 18                              |
| FIGURE 12 - ROACH2 SFP+ MEZZANINE BOARD 19                  |
| FIGURE 13 - VEGAS IF INTERFACE BLOCK DIAGRAM                |
| FIGURE 14 - IF INTERFACE CONTROL BITS 21                    |
| FIGURE 15 - VEGAS SHIELDED RACK TEMPERATURE 25              |
| FIGURE 16 - VALON 5007 RFI ENCLOSURE                        |
| FIGURE 17 - VALON 5007 RFI BOX INTERNAL WIRING 27           |
| FIGURE 18 - VEGAS FIRST LIGHT (FIGURE 1) 29                 |
| FIGURE 19 - VEGAS FIRST LIGHT (FIGURE 2)                    |
| FIGURE 20 - VEGAS FIRST WIDEBAND OBSERVATION                |



1 Introduction and Scope

#### 1.1 Scope

This document summarizes the general design of the <u>VE</u>rsatile <u>GBT Astronomical Spectrometer</u> (VEGAS). This document includes the shielded rack design, the roach2 configuration, the IF modules, the power supplies, and the various components required to interface and interconnect the parts of VEGAS.

Not included in this document is detailed information on the Simulink models, the firmware design and architecture, switching signal generation, the GPU code, or the higher level software.

#### 1.2 Introduction

NRAO in collaboration with the Center for Astronomy Signal Processing and Electronics Research (<u>CASPER</u>) at the University of California, Berkeley (<u>CICADA</u> collaboration) is building an advanced multi-beam spectrometer for the GBT. The National Science Foundation Advanced Technologies and Instrumentation (NSF-ATI) program is funding the new spectrometer project through award number 1006509, "Advanced Multibeam Spectrometer for the GBT".

In this collaboration, the CASPER group is responsible for the FPGA firmware development and GPU software development. The NRAO staff is responsible for the hardware design and packaging, switching signal distribution, and the high level software to integrate VEGAS into the existing GBT M&C system.

VEGAS will replace capabilities of the existing spectrometers and will support data processing from focal plane array systems. Thus the capabilities of the spectrometer will be synergetic with the multi-pixel camera development program for the GBT. In the present design, the spectrometer will be capable of processing up to 1.25 GHz bandwidth from 8 dual polarized beams or a bandwidth up to 10 GHz from a dual polarized beam.

VEGAS development began in August of 2010 and the first on-sky experiments using the GBT were conducted in December of 2011. These experiments were conducted using a Roach1 based implementation of VEGAS. First wideband mode experiments were conducted in March of 2012. These experiments are discussed in section 7.

The production version of VEGAS, including Roach2 boards and 5GSPS ASIAA ADC boards, was implemented in December 2012. Other than the high performance computers, this version of VEGAS is considered to be the final version of the hardware, complete with the shielded rack and full complement of Roach2 boards and IF modules.

#### **1.3** Abbreviations and Acronyms

- **1PPS** One Pulse Per Second
- ADC Analog to Digital Converter

|         | VEC AC   | Doc #: VEGAS-001-A-REP                                  |  |  |
|---------|--|---|--|--|
| 1       | * VEGAS  | Date: 2013-02-26  |  |  |
|         | Design Report  | Status: Released<br>Page: Page 6 of 31                  |  |  |
|         |  |   |  |  |
|         |  |   |  |  |
| NRA     |  |   |  |  |
| ASIAA   | Academia Sinica Institute of Astron                                    | omy and Astronhysics                                    |  |  |
|         |  | Academia Sinica Institute of Astronomy and Astrophysics |  |  |
| CASPER  | Collaboration for Astronomy Signal Processing and Electronics Research |   |  |  |
| CICADA  | Configurable Instrument Collaboration for Agile Data Acquisition       |   |  |  |
| EMI     | Electro Magnetic Interference  |   |  |  |
| FPGA    | Field Programmable Gate Array  |   |  |  |
| GBT     | Green Bank Telescope   |   |  |  |
| GSPS    | Giga Samples Per Second  |   |  |  |
| HPC     | High Performance Computer  |   |  |  |
| M&C     | Monitor and Control  |   |  |  |
| NRAO    | National Radio Astronomy Observatory                                   |   |  |  |
| NSF-ATI | National Science Foundation Advanced Technologies and Instrumentation  |   |  |  |
| RAL     | Radio Astronomy Lab  |   |  |  |
| RFI     | Radio Frequency Interference   |   |  |  |
| SSDS    | Switching Signal Distribution System                                   |   |  |  |

- SSDS
- Switching Signal Distribution System VErsatile GBT Astronomical Spectrometer VEGAS

#### 2 Documentation

#### Applicable documents 2.1

| No   | Document Title                                 | Reference       |
|------|--|-----------------|
| AD01 | Valon Synthesizer for VEGAS                    | VEGAS-002-A-REP |
| AD02 | Valon Synthesizer RFI Test Report              | VEGAS-003-A-REP |
| AD03 | VEGAS Analog IF interface                      | VEGAS-004-A-REP |
| AD04 | VEGAS Switching Signal Distribution System     | VEGAS-005-A-REP |
| AD05 | RAL 1PPS Distributor                           | link            |
| AD06 | VEGAS Block Diagram                            | B35215K003      |
| AD07 | VEGAS Shielded Rack Layout                     | B35215K004      |
| AD08 | VEGAS Shielded Rack Cabling                    | B35215S002      |
| AD09 | VEGAS Rack Power Entry Enclosure               | D35215M015      |
| AD10 | VEGAS Rack Top Plate                           | D35215M016      |
| AD11 | VEGAS Fiber Entry Tube                         | D35215M017      |
| AD12 | VEGAS 10MHz Distribution Mounting Plate        | B35215M027      |
| AD13 | VEGAS Roach2 Chassis Board Stop Plate          | B35215M023      |
| AD14 | VEGAS Roach2 Chassis Signal Bracket            | B35215M022      |
| AD15 | VEGAS Roach2 Chassis Power Bracket             | B35215M021      |
| AD16 | VEGAS Roach2 Board Mounting Plate              | B35215M018      |
| AD17 | VEGAS Roach2 Power Supply Chassis Bottom Plate | B35215M024      |
| AD18 | VEGAS Roach2 Power Supply Chassis Side Plates  | B35215M025      |
| AD19 | VEGAS Roach2 Chassis Side Plate B35215M019     |                 |

| NRA  | *<br>/ <br> | VEGAS<br>Design Report            | Doc #:<br>Date:<br>Status:<br>Page: | VEGAS-001-A-REP<br>2013-02-26<br>Released<br>Page 7 of 31 |  |
|------|-------------|-----------------------------------|-------------------------------------|---|--|
| AD20 | VEGAS       | S Roach2 Chassis Top/Bottom Plate |                                     | B35215M020  |  |

#### 2.2 **Reference Documents**

| No Document Title                                       |                              | Reference   |
|---|------------------------------|-------------|
| RD01  | VEGAS Specification Document | link        |
| RD02 Hoffman- Heat Dissipation in Electrical Enclosures |                              | <u>link</u> |

#### **3 VEGAS Electronics Design**

VEGAS is comprised of eight Roach2 Rev2 boards, each containing two ASIAA 5GSPS ADC converter boards. The signal inputs to VEGAS pass through the bulkhead panel at the top of the rack and connect to the analog IF interface modules, which condition the signals before they are connected to the ADC boards.

A Valon 5007 synthesizer is used as the ADC clock source. The synthesizer output is split so that the clock signal can be connected to both ADC boards. The synthesizer accepts an external 10MHz reference to lock it to the GB site timing center.

VEGAS can accommodate the use of switching signals. It can be configured as the master-of or the slave-to external switching signals. A custom switching signal distribution chassis resides in the VEGAS rack to allow these signals to be distributed to the eight roaches, as well as to the receivers and/or backends that use them.

A 1PPS signal enters the rack through the bulkhead panel and connects to a RAL 1PPS distributor that resides in the VEGAS rack. This chassis provides a 1PPS signal to all eight Roach2 boards.

A complete block diagram and rack layout of VEGAS can be found in **[AD 06]** and **[AD 07]**, respectively. The complete VEGAS specifications can be found in **[RD 02]**.

#### 3.1 Roach2 Board

The Roach2 Rev2 board uses the Xilinx Virtex-6 SX475T FPGA. It has the following features:

- Stand-alone PowerPC 440EPx on board to provide control functions.
- 2 x Multi-gigabit transceiver break out card slots, supporting up to 8x10Ge links which may be CX4 or SFP+
- 4 x 36 \* 2M QDR II+ SRAMs connected to the FPGA
- One 72-bit DDR3 RDIMM slot connected to the FPGA
- 2 x ZDOK connectors
- FTDI FT4232H USB to JTAG, serial and IIC

Figure 1 is the basic block diagram of the Roach2 board.

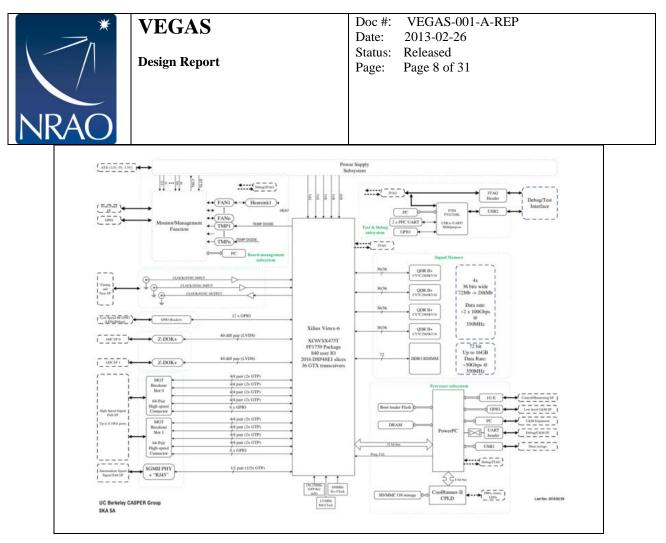


Figure 1 - Roach2 Block Diagram

#### 3.1.1 Uboot Configuration

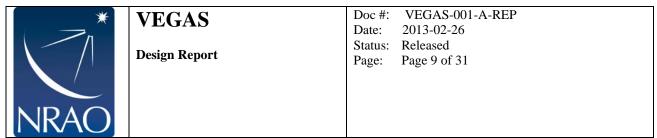
Before using the Roach2 boards in VEGAS, they were configured using the uboot interface. To access the uboot prompt, a USB "A to B" cable is attached to connector P3 on the Roach2 board. This provides a serial connection between the Roach2 board and a computer.

Using a terminal emulator (such as Windows hyperterminal) the Roach2 will be connected to COM12, or similar. Using the terminal, the bootup text can be observed after power-up. Shortly after power-up, the user is prompted to press any key to interrupt the boot. Doing so will provide access to the uboot prompt.

From the uboot prompt, each Roach2 was given a unique MAC address for the 1GbE interface of the power PC and configured to boot from the network using the following commands:

```
setenv ethaddr 02:44:01:xx:yy:zz
set bootcmd run netboot
saveenv
```

The Roach2 will use the given MAC address and attempt to boot from the network on the next boot cycle. For VEGAS, the Roach2 boards all use the machine "tofu" as the boot host.



The MAC address scheme is 02:44:01:xx:yy:zz, where xxyyzz is the last six digits of the Roach2 board's serial number.

Here is a listing of the VEGAS Roach2 board names, MAC addresses and IP addresses:

| vegasr2-1 | 02:44:01:02:06:20 | 10.16.98.140 |
|-----------|-------------------|--------------|
| vegasr2-2 | 02:44:01:02:06:13 | 10.16.98.141 |
| vegasr2-3 | 02:44:01:02:06:16 | 10.16.98.142 |
| vegasr2-4 | 02:44:01:02:06:11 | 10.16.98.143 |
| vegasr2-5 | 02:44:01:02:06:15 | 10.16.98.144 |
| vegasr2-6 | 02:44:01:02:06:12 | 10.16.98.145 |
| vegasr2-7 | 02:44:01:02:06:19 | 10.16.98.146 |
| vegasr2-8 | 02:44:01:02:06:18 | 10.16.98.147 |

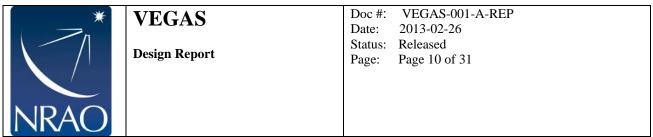
#### **3.1.2 I2C Communications**

The I2C bus is used by the Roach2 to communicate with the IF module, in order to configure the different filters and noise source settings. I2C bus 0 is used for this and the IF modules are all set to use address 0x38.

In order to test if this functionality is working, there are a few I2C commands built into Linux on the Roach2. For instance to scan the bus to make sure the IF module is present, log into the Roach2 as root and use the i2cdetect command as shown in Figure 2. Note that address 0x38 is present in the list.

```
🛃 prospero.gb.nrao.edu - PuTTY
                                                                      <u>- 0 ×</u>
root@vegasr2-8:~#
root@vegasr2-8:~#
root@vegasr2-8:~# i2cdetect 0
WARNING! This program can confuse your I2C bus, cause data loss and worse!
I will probe address range 0x03-0x77.
Continue? [V/n] y
0 1 2 3 4 5 6 7 8 9 a b c d e f
. 00
                                  -- Oc
           -- -- -- -- -- -- -- -- --
30:
      -- -- -- -- -- 38 -- -- -- -- --
      40:
50: UV UV -- -- 54 55 -- -- -- -- -- --
root@vegasr2-8:~#
```

Figure 2 - Roach2 I2C Bus Detect Test



Other commands are available for reading and writing such as i2cget and i2cset.

Special cabling is required to connect the IF modules to the Roach2 to use the I2C. The cable is actually comprised of two cables. One cable connects Roach2 P7 to "bracket 1" [**AD 14**] on the Roach2 mounting plate. Then another cable connects from "bracket 1" to the IF module. Details of this cable are shown in Figure 3 below, as well as [**AD 08**].

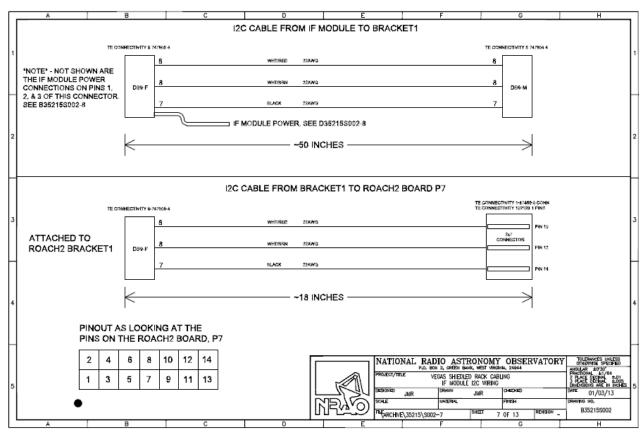
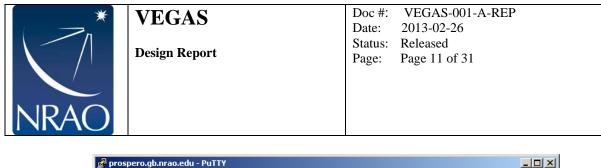


Figure 3 - VEGAS I2C Cabling

#### **RS232** Communications

The serial port ttyS1 is used by the Roach2 to communicate with the Valon synthesizer, in order to control and monitor several parameters such as output frequency, reference select, lock status, output level, and some others.

The python program for communicating with the Valon is loaded into the Roach2 and can be accessed via logging into the Roach2 as root. Figure 4 below shows how to load python and check the output frequency, the phase lock status, and the reference select. There are a number of other commands for interfacing with the Valon.



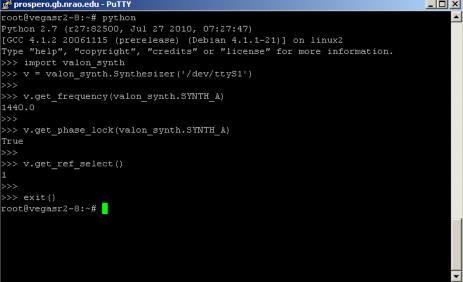


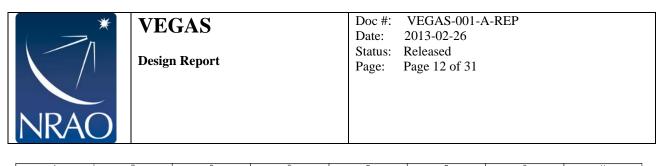
Figure 4 - Python Interface for Valon Synthesizer

The default mode is for ttyS1 is to present a login prompt after bootup. In order to ensure that this wouldn't cause problems with the Valon synthesizer, the login prompt was disabled by editing the file **/etc/inittab** and commenting out the following line:

```
#T1:23:respawn:/sbin/getty -L ttyS1 115200 vt100
```

After the next reboot, the Roach2 will not issue a login prompt on ttyS1.

Special cabling is required to connect the Valon synthesizer 9-pin D-connector to the Roach2 P6 connector, to use the serial port. Details of this cable are shown in Figure 5 below, as well as **[AD 08]**.



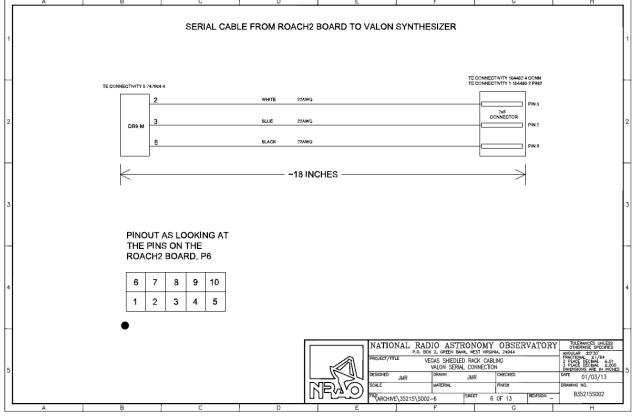
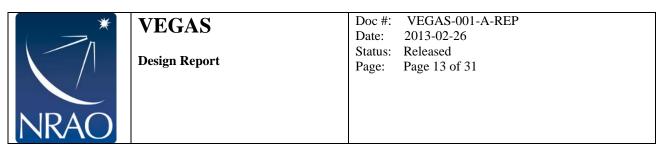


Figure 5 - VEGAS RS232 Cabling

#### 3.1.3 Front Panel I/O

There are a few signals from the front panel I/O brought out to "bracket 2" **[AD 15]** on the Roach2 plate. The first is a momentary rocker switch used to power on and off the Roach2 board. Next is a green LED that indicates "power on" and the last is a red LED that indicates the status of "CPU\_RDY". These signals are all connected to the Roach2 board via connector P16.

Figure 6 shows the details of these connections.



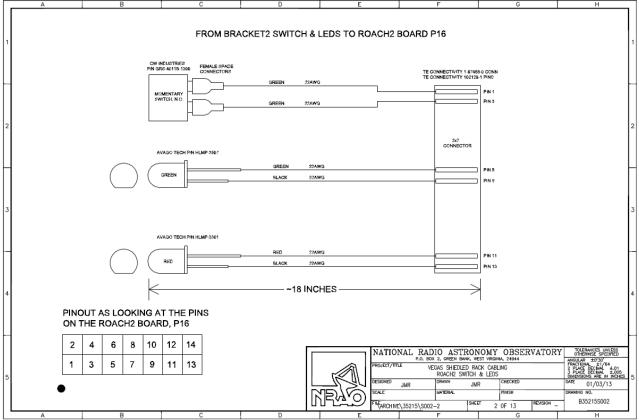


Figure 6 - VEGAS Front Panel I/O Cabling

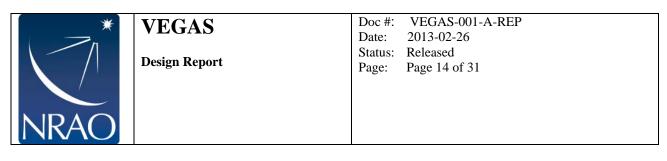
#### 3.1.4 Switching Signal Cabling

Several levels of cabling are required to accommodate the use of switching signals in VEGAS. On the Roach2, connectors P13 and P15 are used to get the switching signals in and out of the board. Incoming signals to all of the Roach2 boards connect to P13. Outgoing signals from the master Roach2 connect to P15.

The switching signals to and from the Roach2 all travel on a 20-position ribbon cable. Similar to the I2C cabling, there are two cables required to connect the switching signals to the SSDS. One that connects from either P13 or P15 to a connector on "bracket 1" and another that connects from "bracket 1" to the SSDS.

Note that the SSDS chassis has labels like "TO SLAVE n J2" and "TO MASTER J9". This is because the SSDS was built with the Roach1 connector labeling in mind. The equivalent GPIO headers on the Roach2 boards are P13 and P15.

Details of these cables are shown in Figures 7, 8, and 9 below, as well as [AD 08].



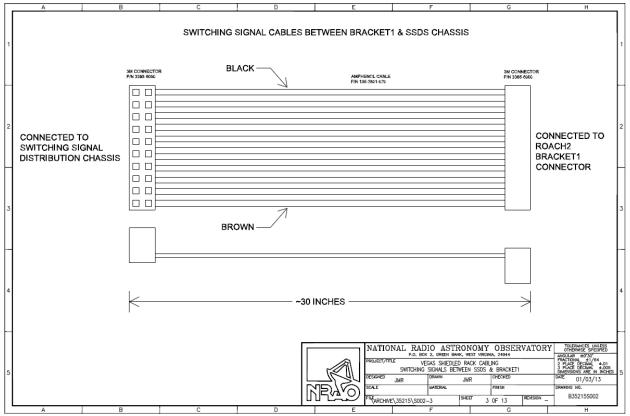
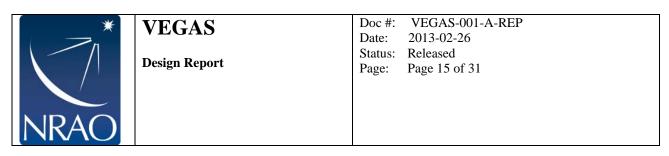


Figure 7 - Switching Signal Cabling, Bracket 1 to SSDS



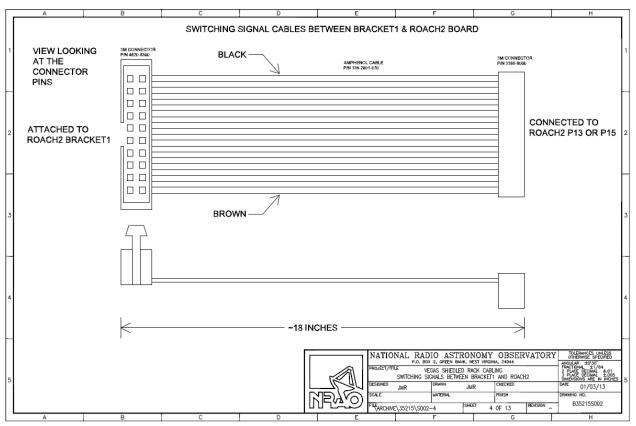
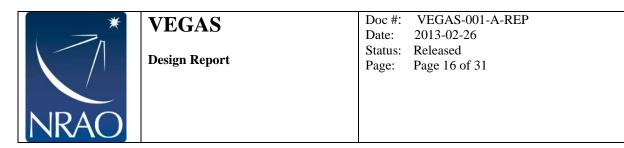
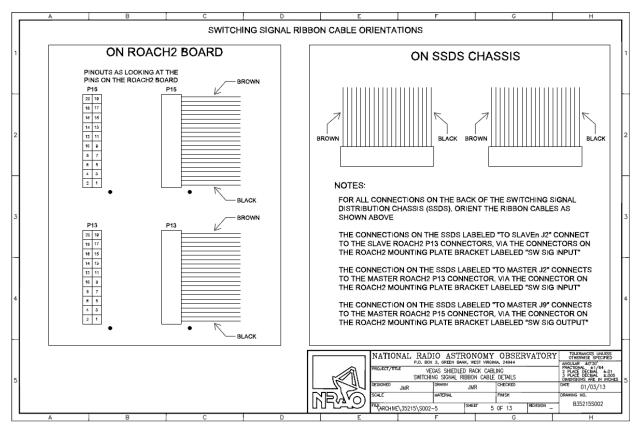


Figure 8 - Switching Signal Cabling, Bracket 1 to Roach2





**Figure 9 - Switching Signal Cabling Details** 

#### 3.1.5 Network Connection

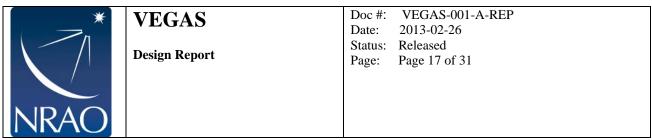
The network connection to the Roach2 is a simple RJ45 patch cable connected from connector P9 (labeled PPC NET) to the 1GbE ethernet switch which resides in the rack.

The network switch receives its uplink connection using a fiber optic adapter and a duplex LC/LC fiber cable.

#### 3.1.6 Power Supply

For typical Roach2 applications, the board is delivered pre-installed in a 1U chassis that contains a standard computer power supply. Given that the plan was to install the Roach2 boards in a custom vertical-mount chassis, the VEGAS boards were shipped without a chassis and power supply.

The Roach2 boards in VEGAS each utilize a small 120W PicoPSU power supply unit. This unit attaches directly to the ATX connector on the Roach2 and is powered by a single +12VDC supply.



To provide +12VDC to the eight PicoPSU units, a set of three 500W switching power supplies are installed at the bottom of the rack. The first two supplies provide power to three roaches each, and the third supply powers the last two.

There is a Molex connector on "bracket 2" of the Roach2 mounting plate that provides the input for power from the DC power supply chassis. There is a 15A fuse on the Roach2 plate for this power connection. This +12V supply also provides power to the Valon synthesizer. Details of the power wiring are shown in Figure 10 below, as well as [AD 08].

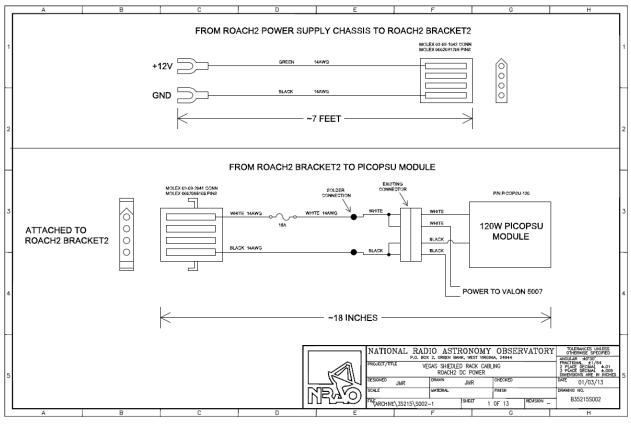


Figure 10 - Roach2 Power Supply Wiring

### 3.2 ASIAA 5GSPS ADC Board

VEGAS uses the 5GSPS V2.0 DMUX 1:1 ADC board developed by the group at ASIAA. This board attaches to the Roach2 ZDOK connectors and converts the input signal to 8-bit samples.

The ADC board has four SMA connectors for attaching the IF inputs (I and/or Q), the ADC clock, and the sync (1PPS) signal. There are two of these boards per Roach2 in VEGAS. Figure 11 below is an image of the board, with the SMA connectors labeled.



Design Report

Doc #: VEGAS-001-A-REP Date: 2013-02-26 Status: Released Page: Page 18 of 31



Figure 11 - 5GSPS ADC Board

### 3.2.1 ADC clock

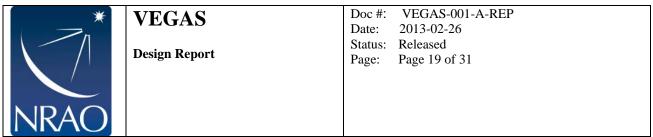
Each of the ADC boards require an ADC clock signal input. The source of this signal is the Valon synthesizer which is installed on the Roach2 mounting plate. The SYN1 output is used to provide the clock signal to both ADC boards. The Valon output is split using a Mini Circuits ZX10-2-20-S+ power divider. All of the ADC clock signals travel on RG402 semi-flex SMA coax cables **[AD 08]**.

### 3.2.2 1PPS

VEGAS uses the site timing center 1PPS signal to sync the Roach2 boards together when taking data. This signal comes in through the bulkhead top plate of the rack and connects to the input of the RAL 1PPS distributor. Outputs from this distributor are connected to each of the eight Roach2 boards. The signal enters the Roach2 board through the ADC board attached to ZDOK 0. The 1PPS signals travel on LMR-195 BNC cables from the 1PPS distributor to a bulkhead connector on "bracket 1" of the Roach2 mounting plate. From there, it is adapted to an RG188 SMA cable and connected to the ADC "sync" input.

#### 3.2.3 IF input

The IF inputs from the GBT come in through the bulkhead plate at the top of the rack, and connect to the IF module inputs on the front-side of the rack. From the IF module outputs on the back-side of the rack, the signals connect to the "I input" of the ADC boards, through 6dBm pads, already attached to the ADC inputs. The IF signals travel on RG402 semi-flex SMA coax cables [AD 08].



Typically, systems that utilize CASPER hardware use CX4 cables to connect the 10GbE between the FPGA board and a computer. Since the VEGAS hardware is installed in a shielded enclosure and the HPC machines are outside of this enclosure, it is impossible to use copper cables for the 10GbE connections between the two due to the filtering required.

To solve this problem, fiber optic cables are used to connect the 10GbE. To do this, the SFP+ mezzanine board is used on the Roach2. This board contains four SFP+ ports and if used in conjunction with a 10GbE SFP+ fiber adapter then the 10GbE connection can be made using a duplex LC/LC fiber cable. VEGAS uses "CH0" of the SFP+ mezzanine board. The board itself is attached to the "Mezzanine 1" slot on the Roach2.

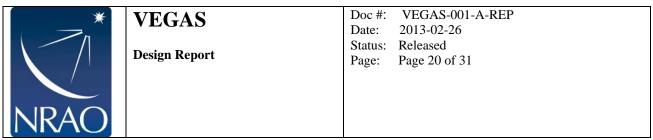
Figure 12 below shows the SFP+ board with the channels labeled.



Figure 12 - Roach2 SFP+ Mezzanine Board

### 3.4 Valon Synthesizer

Each Roach2 board in VEGAS has a dedicated Valon 5007 dual synthesizer unit to provide the clock to the ADC boards. The 5007 has two RF outputs that have a range of 137.5 MHz to 4400 MHz. It can accept an external reference frequency, or use its own internal reference. The output level can be adjusted to 0, +3, +6, or +8dBm. It also has on-board flash that can retain the desired settings when power cycled.



There is a serial interface adapter board for the 5007 that allows users to remotely adjust the various parameters of the unit, which makes it very useful for VEGAS because of the need to change the ADC clock rate.

#### 3.5 Analog IF Interface

The IF modules **[AD 03]** condition the signals from the GBT IF system to make them suitable for VEGAS. Level adjustment and anti-aliasing filtering are the primary functions, and the interface also provides test features such as test tone injection capability, input signal monitoring and a built-in noise source correlated for each pair of channels.

Figure 13 is a block diagram of the IF interface.

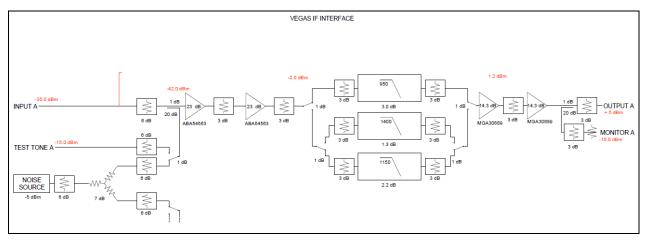


Figure 13 - VEGAS IF Interface Block Diagram

The top of the diagram shows the main signal path from the GBT IF system to the input ports of the Roach2 ADCs. Attenuators are used to improve the matching between the cables, the amplifiers, the filter and the ADC input. A coupler is used to inject either noise highly correlated between channels or other test signals brought in by connectors from the outside. A switching scheme selects one of three anti-aliasing filters. Another pair of couplers provides a point to monitor the signals immediately before they go in to the Roach2 ADCs.

To select the different filters and enable/disable the noise source, there are five control bits per pair of channels. Switching of the five bits is accomplished using I2C port 0 on the Roach2 board. There is a PCF8574A I/O 8-bit I/O expander in the IF module. This device is set to use address 0x38. Bits 0-4 are connected to control bits 1-5 respectively.

The function of the control bits is shown in Figure 14 below.

|--|

| Bit | Channel | Function     | 1 =  | Comment          |
|-----|---------|--------------|------|------------------|
| 0   | Both    | Noise On/Off | Off  |                  |
| 1   | 1       | Noise/Tone   | Tone |                  |
| 2   | 2       | Noise/Tone   | Tone |                  |
| 3   | Both    | 950/Wide     | Wide | Wide = 1400/1150 |
| 4   | Both    | 1400/1150    | 1400 |                  |

Figure 14 - IF Interface Control Bits

Upon power-up, all bits default 1, making the default configuration 1400 MHz, wide mode, noise source off, tone input state.

#### 3.6 Switching Signal Distribution System

The Switching Signal Distribution System for VEGAS **[AD 04]** is a custom electronics package designed at NRAO GB. It was developed specifically for distributing signals from a master Roach board to as many as eight slave Roach boards and to the switching signal mux in the GBT equipment room. It was also designed to accommodate external switching signals from another source, and distribute those signals to the Roach boards.

The SSDS distributes four different switching signals – Advanced SIG/REF, SIG/REF, CAL, and BLANK.

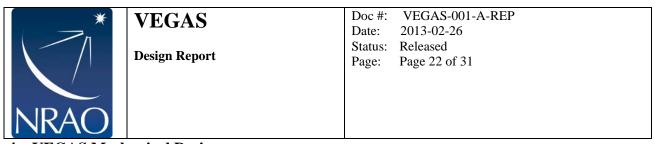
#### 3.7 RAL 1PPS Distributor

The RAL 16-channel 1PPS Distributor [**AD 05**] developed at UC Berkeley is used in VEGAS to distribute the site 1PPS signal to all eight Roach2 boards. This unit receives 1PPS in and drives the 16 outputs simultaneously at LVTTL levels, when terminated at 50ohms. The rise/fall time of the output signals are approximately 1.6ns.

#### 3.8 10MHz Distribution

Since every Roach2 in VEGAS has a dedicated Valon synthesizer, each of them requires a 10MHz signal to provide the reference to phase lock the Valon to the site timing center.

It turns out that a simple 8:1 power divider is sufficient for distributing the 10MHz signal to the Roach2 boards. The 10MHz signal enters the VEGAS rack, on an LMR-195 BNC cable, at the bulkhead top plate, and connects to the power divider. From there, RG188 SMA cables connect to SMA bulkhead connectors on "bracket 1", and then to the Valon synthesizer box. Details of these cables can be found in **[AD 08]**.



#### 4 VEGAS Mechanical Design

This section describes the mechanical design of VEGAS.

#### 4.1 Shielded Rack Top Plate

A custom top plate **[AD 10]** for the rack was fabricated to replace the plate that came with the rack. This was mainly to accommodate all of the connectors needed to get signals in and out of the rack, along with the fiber optic tube. The location and hole pattern for the honeycomb filter was retained.

The plate contains 32 SMA bulkhead connectors. 16 are used to connect the IF signals and the other 16 are available for various uses such as test tone inputs and monitor outputs. As-built, 16 were connected for the incoming IF signals and two were cabled up inside the rack to be used for test tone inputs as needed.

There are also 10 BNC bulkhead connectors. Two of them are used for the timing signals 10MHz and 1PPS. Five of the others are used for switching signals.

There is a fiber optic choke tube [AD 11] to allow fiber cables to enter the rack.

#### 4.2 Shielded Rack Power Entry

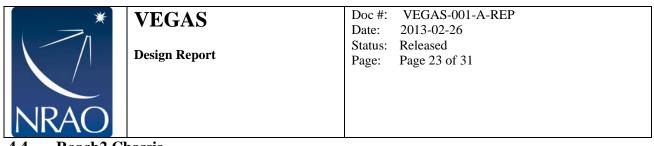
AC power enters the rack through a power entry box **[AD 09]** which is a welded aluminum enclosure. This enclosure is comprised of a so-called "dirty side" and "clean side" and there are filters between them to maintain the RFI barrier of the rack.

#### 4.3 Roach2 Mounting Plate

The Roach2 boards and their ADC boards are mounted on a custom aluminum plate **[AD 16]** which is designed to mount vertically and slide into a custom Roach2 chassis. Mounting them vertically allows for better cooling as the air flows up through the rack. Also mounted to that plate are the Valon synthesizer, the ADC clock power divider, a fuse for the incoming +12V power, and two brackets.

One of the brackets, referred to as "bracket 1", contains connectors for switching signals, I2C, 10MHz, and 1PPS and "bracket 2" contains the power connector, power switch, and two LEDs.

This plate was designed to be a fully contained Roach2 assembly to make testing and troubleshooting on the bench easier. Most of the signals in and out of the board are connected to the bracket connectors, meaning very little needs to be disconnected from the Roach2 board to remove it from the rack. The only connections directly to the Roach2 board (network, 10GbE, and IF connections) are easy to remove.



4.4 Roach2 Chassis

There are two identical aluminum chassis' **[AD 19]**, **[AD 20]** in VEGAS that are designed to hold five Roach2 board plates each. Given that VEGAS uses eight Roach2 boards, they are arranged four per chassis in the rack.

The top/bottom plates have large open slots to allow airflow through the chassis.

The Roach2 mounting plates are designed so that the board itself is inset from the front of the rack, to allow for sufficient room to connect the fiber cable with a safe bend radius.

There are board stop plates **[AD 13]** mounted to the bottom of the chassis', front and back, to keep the Roach2 boards from sliding out of the chassis as cables are connected.

#### 4.5 IF Module Chassis

The IF modules are mounted in a commercial 1U chassis and are arranged two per chassis, with the IF inputs from the converter rack available at the front of the VEGAS rack. The outputs of the module, which connect directly to the ADC boards, are on the back side.

#### 4.6 Network Switch

Similar to the way the Roach2 boards are inset from the front of the rack, custom mounting brackets were designed to inset the network switch. They are made of stainless steel to provide a little more strength because they hold the entire weight of the switch.

#### 4.7 Roach2 Power Supply Chassis

The Roach2 power supply units are installed in a custom 1U chassis **[AD 17]**, **[AD 18]** that is mounted at the bottom of the rack on the front side.

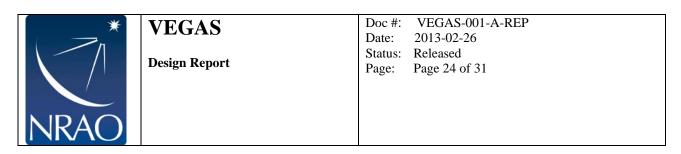
#### 5 Thermal Analysis

This section describes some of the thermal considerations and measurements made on the VEGAS hardware.

#### 5.1 Shielded Rack Heat Calculations

The thermal properties of the shielded rack were calculated based on the estimated heat dissipation of the hardware and the airflow of the ventilation/blower assembly that came installed in the rack as purchased.

The power dissipation is estimated to be a maximum of 1500W. The blower assembly is specified to provide 400cfm. With the rack doors closed and only the UPS installed, this level of airflow was confirmed using a small handheld airflow meter at the top of the rack.



The following calculations are based on those in the "Fans and Blowers" section of the document "Heat Dissipation in Electrical Enclosures" published by Hoffman [**RD 02**].

According to this document:

**CFM = (3.16 \* WATTS) /** 

where,

 $CFM = Airflow through the rack, in ft^3/min$ 

WATTS = Internal heat load, in watts

 $\triangle T$  = Internal temperature minus ambient temperature, in °F

Assuming the desired temperature rise is 20°F above ambient,

CFM = (3.16 \* 1500) / 20 CFM = 237 cfm

This result means that if the airflow through the rack can remain above 237cfm with the full complement of hardware installed, then cooling should not be an issue.

Once all of the hardware was installed in the rack, the airflow was re-measured at the top of the rack to be unchanged from the empty rack.

During early testing, a two-channel temperature logger was placed inside the rack to verify the temperature was sufficiently cool. One channel was measuring the temperature at the bottom (intake) of the rack and the other was measuring the temperature at the top (exhaust) of the rack. Figure 15 shows the results of the temperature logger data. The max temperature measured was around  $34^{\circ}$ C which is a safe operating temperature for the hardware.



Design Report

Doc #:VEGAS-001-A-REPDate:2013-02-26Status:ReleasedPage:Page 25 of 31

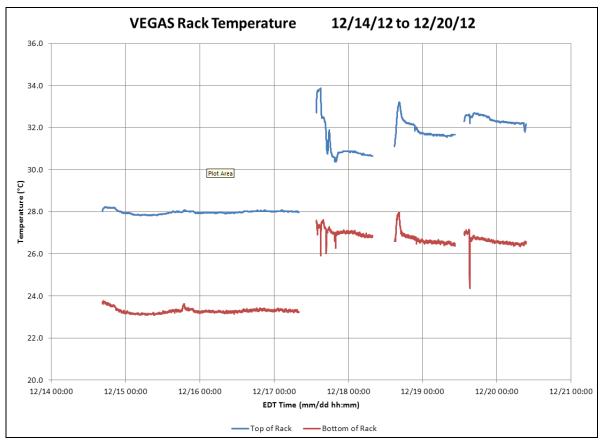


Figure 15 - VEGAS Shielded Rack Temperature

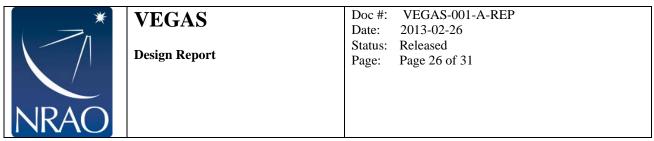
#### 5.2 10GbE PHY Chip Temperature

There was some concern about the temperature of the PHY chip on the SFP+ mezzanine cards. The Vitesse design guide states:

"For typical applications, the VSC8486 can be operated in an ambient temperature environment of +80 degrees C with no airflow and without a heatsink."

As shown above, the maximum temperature measured inside the VEGAS rack was around 34°C, so the ambient temperature environment is sufficient to meet the above criteria.

Other datasheets mention that the maximum specification for the case temperature is 85°C. The temperature of the PHY chips in VEGAS was measured using an infrared viewer to be around 60°C. One thing to note is that the datasheets available were for the VSC8486 and the SFP+ boards actually use the VSC8488 so the assumption was made that the thermal specifications between the two chips are the same.



#### 6 **RFI/EMI** Considerations

Given the large amount of RFI generated by the Roach2 board, it was required to install them inside of a shielded rack, despite the fact that VEGAS will reside in the shielded GBT equipment room. Several things had to be considered to successfully shield the noisy digital electronics of VEGAS.

#### 6.1 Shielded Rack

It was decided that the best method of shielding VEGAS would be to install it in a shielded rack. As opposed to trying to develop a shielded enclosure for each of the Roach2 boards.

#### 6.1.1 AC Power Entry

AC power enters the rack through an RFI tight enclosure **[AD 09]** mounted on the side of the rack. The power enters the "dirty side" of the enclosure through a twist lock connector, through a circuit breaker, and then connected to a terminal strip. There are connections from the terminal strip, through cylindrical RFI filters to the "clean side" of the enclosure, where it enters the rack through a hole. There are o-ring type RFI gaskets at the interface between the enclosure and the rack, and between the enclosure and its lid.

#### 6.1.2 Rack Top Plate

The top plate of the shielded rack **[AD 10]** was designed to allow signals in and out, but still be compliant with respect to the RFI requirements. The SMA and BNC connections all utilize fully shielded cables for the interconnects. The unused connectors are capped off. There is a fiber optic tube (waveguide beyond cutoff) **[AD 11]** utilized to get the 10GbE and 1GbE network connections in and out of the rack. Finally, the original honeycomb filter that came with the rack was retained to allow airflow.

#### 6.2 Valon Synthesizer

An RFI enclosure **[AD 01]** was developed to house the Valon 5007. One reason was because this unit is used in other projects at Green Bank, so it was required to reduce the RFI emissions from the Valon. But, more importantly for VEGAS is to reduce the emissions since it is mounted so close to the sensitive RF inputs of the ADC boards.

The RFI enclosure consists of a custom aluminum housing with an RFI-gasketed aluminum lid. Tubular feedthru pi filters are used to bring +12VDC into the box. A filtered DB-9 connector is used for the RS232 connection. The RS232 adapter boards were custom ordered from Valon Technology with the filtered DB-9 connector in place of the standard connector. NRAO provided Valon Technology with the connectors prior to placing the order.



VEGAS Design Report Doc #:VEGAS-001-A-REPDate:2013-02-26Status:ReleasedPage:Page 27 of 31

SMA bulkhead connectors are used for the reference input and RF outputs of the 5007. Fully shielded cables are used to connect to these ports, and any unused ports are capped off with a 500hm terminator.



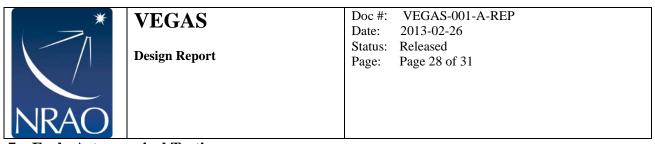
Figure 16 - Valon 5007 RFI Enclosure

In order to install the 5007 in this RFI enclosure, it was custom ordered with the SMA connectors removed. This allows the board to be installed in the enclosure with one end of a pigtail coax cable soldered to the 5007 board and the other end connected to the bulkhead connector with a normal SMA connector. Figure 17 below shows the internal wiring.



Figure 17 - Valon 5007 RFI Box Internal Wiring

An RFI test was performed on this assembly, in the anechoic chamber at NRAO GB, and it was found that there were no detectable emissions from the unit [AD 02].



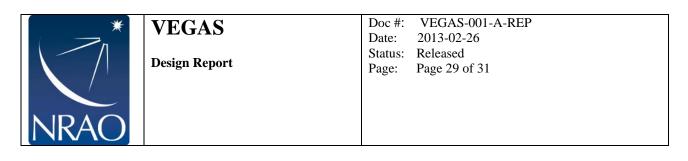
7 Early Astronomical Testing

The VEGAS first light experiment was conducted in December of 2011. The following text and images were generated by Glenn Jones (NRAO/Caltech) and were published in the February 1, 2012 issue of the NRAO eNews newsletter.

A prototype version of the new Versatile GBT Astronomical Spectrometer (VEGAS) saw first light 16 December 2011 at the Green Bank Telescope. VEGAS is designed to harness the power of the new K-band Focal Plane Array by providing digital spectroscopy on up to eight dual-polarization inputs, each with a total bandwidth of up to 1.25 GHz. The instrument will be built with CASPER ROACH II FPGA boards feeding a cluster of GPU-enabled computers. These initial tests were performed with just a single feed at L-band to demonstrate the spectrometer.

Figures 1a and 1b show a drift-scan observation of neutral hydrogen. Figure 1a shows the spectrum from the eight 12.5 MHz sub-bands which are produced by the FPGA and then further channelized into 4096 channels by the GPU for a final resolution of ~3 kHz. A resonance in the L-band receiver can be seen around 1447 MHz, and some artifacts from interference are present in the sub-band above 1490 MHz. Figure 1b shows the detail of the hydrogen line and a crude drift-scan map of the data. The final system will provide eight independently tunable sub-bands.

In addition to high-resolution spectroscopy, VEGAS will also be capable of producing at least 1024 channels across the full 1.25 GHz band and supports integration times as short as 0.5 milliseconds, enabling wide bandwidth pulsar searches. Figure 2 shows a folded phase-frequency profile of the bright pulsar B0329+54. Filters in the receiver limit this test observation's bandwidth. The dispersion sweep of the pulsar is clearly visible. Horizontal lines are caused by interference, while peaks and nulls in the pulsar spectrum are caused by interstellar scintillation and the receiver gain response.



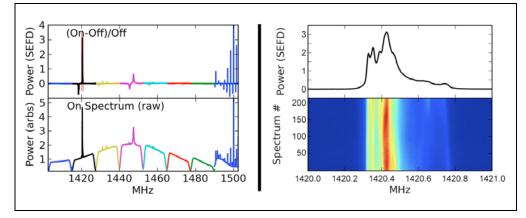


Figure 18 - VEGAS First Light (figure 1)

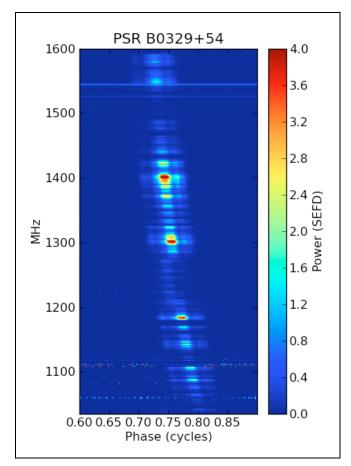
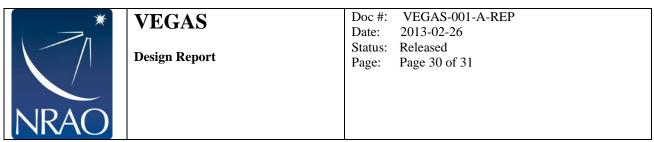


Figure 19 - VEGAS First Light (figure 2)



The VEGAS first wide bandwidth observations were conducted in March of 2012. The following text, and first light image, was generated by Glenn Jones (NRAO/Caltech) and Andrew Siemion (UC Berkeley) and was published in the May 3, 2012 issue of the NRAO eNews newsletter.

*Rapid development of the new Versatile GBT Astronomical Spectrometer* (VEGAS) continues. This past March, the VEGAS team, including local NRAO staff and members from UC Berkeley and West Virginia University, met in Green Bank to test an expanded prototype of the system. Eight ROACH FPGA boards and eight host computers were assembled to perform extensive system integration tests as well as to test and characterize the wide bandwidth capabilities that the spectrometer will provide. Test observations were performed to demonstrate the ability to process the entire 8 GHz band (spanning 18 to 26 GHz) provided by the central beam of the K-band Focal Plane Array (KFPA). In the present configuration, each ROACH board produces a 1024-channel, full Stokes spectrum with 1300 MHz of usable bandwidth. Thus the whole system can provide an aggregate bandwidth greater than 10 GHz. The spectrometers support integration times as short as 500 microseconds. Test observations were made on the bright pulsars B0355+54 and B0329+54 (see Figure) to demonstrate the utility of the system for high frequency, wide bandwidth pulsar observations. This high frequency pulsar capability will be used to perform the most sensitive search yet for pulsars near the galactic center. The sensitivity of the KFPA and the spectrometers was also measured on the continuum calibrator source DR21. Development of the high-resolution spectral line modes will continue through the summer.



Design Report

Doc #:VEGAS-001-A-REPDate:2013-02-26Status:ReleasedPage:Page 31 of 31

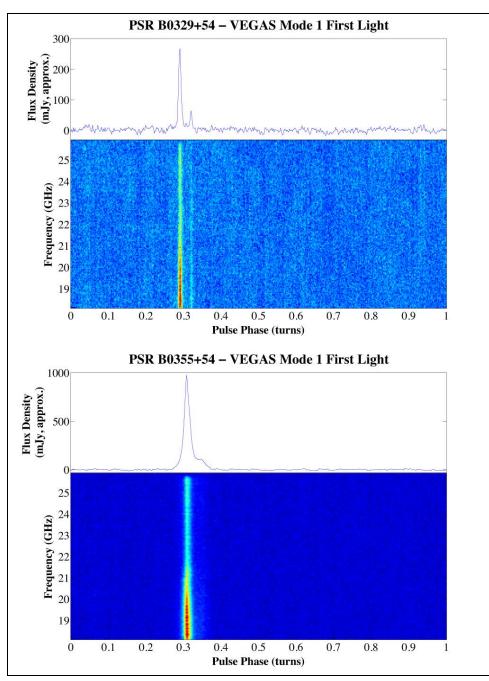


Figure 20 - VEGAS First Wideband Observation