REQUIRED FUNCTIONALITIES . . .

1.0) Lite RPC Server including . . .
- 1.1) Full instrument configuration / control
- 1.2) Self test
- 1.3) Health / Status monitoring
- 1.4) Expert User "Scope" capabilities

2.0) PSRFITS Formatter
3.0) PFB / FIR
4.0) Power
5.0) Full Stokes
6.0) Coherent De-dispersion including . . .
- 6.1) Sub-banding segmentation
- 6.2) FFT
- 6.3) ISM^{-1} multiplication
- 6.4) FFT^{-1}
- 6.5) Sub-banding re-integration
- 6.6) Tempo2 / POLYCOs management

7.0) Period folding (on multiple sources if possible)
8.0) Vector accumulation

POL 0 (1,024 MHz)
SYNCH
"I" IN
CLK "I"
(2,048 MSPS)
ADC 0
(INTERLEAVED)
ZDOK ZDOK
16.4Gb
DMUX
iBOB FPGA
(256 MHz)
iBOB 0
8.2Gb XAUI 8.2Gb
8.2Gb XAUI 8.2Gb

POL 1 (1,024 MHz)
SYNCH
"I" IN
CLK "I"
(2,048 MSPS)
ADC 1
(INTERLEAVED)
ZDOK ZDOK
16.4Gb
DMUX
iBOB FPGA
(256 MHz)
iBOB 1
8.2Gb XAUI 8.2Gb
8.2Gb XAUI 8.2Gb

1 PPS
CX (1,024 MHz) (↑↓)

CX4 ... 8.2Gb XAUI

5.0GB/s

3.4GB/s DDR2 / DDR2 3.4GB/s (multiple rows)

User FPGA 3
User FPGA 4
2.5GB/s
Cont FPGA
DDR2 3.4GB/s
10Ge
10/100Me
5.0GB/s
User FPGA 2
User FPGA 1
10Ge ... 10 Gb

BEE2

NOTES . . .

1) In order to handle two polarizations at up to 1 GHz (2GSPS at 8 bits), we'll need two iADCs and two iBOBs as depicted

2) The two iADCs will be operated in their "interleaved" modes (conversions on both leading and trailing edges of their convert clocks), and will receive 1PPS as a basic system synch signal

3) The two iBOBs will simply serve as "De-MUXING" devices to divide the requisite data throughput into a total of four XAUI channels (each at 8.2Gbps) as shown

4) The block diagram of the BEE2 is intended to offer a simplified depiction of its internal infrastructure and the various data paths (and data rates) available. The intent here is to offer a way to visualize how best to divide up and place the requisite functionalities listed to the right above.

5) Note that, within the BEE2, data can be transferred directly between the USER FPGAs in a "RING" fashion (1 - 2, 2 - 3, 3 - 4, and 4 - 1) at a sustained rate of 5.0 GBYTES / sec; and that each USER FPGA can transfer data to / from the CONTROL FPGA at a sustained rate of 2.5 GBYTES / sec. In addition, each FPGA can support a total of four 72-bit wide DDR2 modules with an effective (aggregate) sustained data rate of 3.4 GBYTES / sec per module.

NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, WV 24944

DESIGN BY:	DATE:	TITLE:
DRAWN BY: Randy L. McCullough	DATE: 18-SEP-07	PROPOSED ARCHITECTURE TEMPLATE
CHECKED BY:	DATE:	

| SHEET: 1 of 1 | DRAWING NUMBER: TBA | REV: A | SCALE: NONE |