1. In order to handle two polarizations at up to 1 GHz (200 kSPS at 8 bits), we need two ADCs and two 8-bit DACs as depicted.

2. The two ADCs will be operated in their "interleaved" modes (conversions on both leading and trailing edges of their convert clocks), and will receive 1PPS as a basic system sync signal.

3. The two 8-bit DACs will simply serve as "Demultiplexing" devices to divide the receive data throughput into a total of four 32-bit channels (each at 800 kSPS) as shown.

4. The block diagram of the BEE2 is intended to offer a simplified depiction of its internal infrastructure and the various data paths (and data rates) available. The intent here is to offer a way to visualize how the system works and place the required functionalities listed to the right above.

5. Note that, within the BEE2, data can be transferred directly between the USER FPGA and the "RING" fashion (1-2, 3-4, and 5-6) at an assumed rate of 5.0 GBYTES/sec, and that each USER FPGA can send data from the CONTROL FPGA at an assumed rate of 2.5 GBYTES/sec. In addition, each FPGA can support a total of four 20-bit wide 8-bit modules with an effective (aggregate) sustained data rate of 3.4 GBYTES/sec per module.