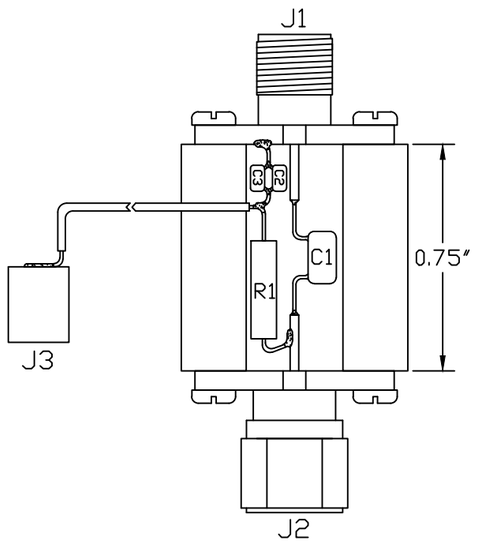
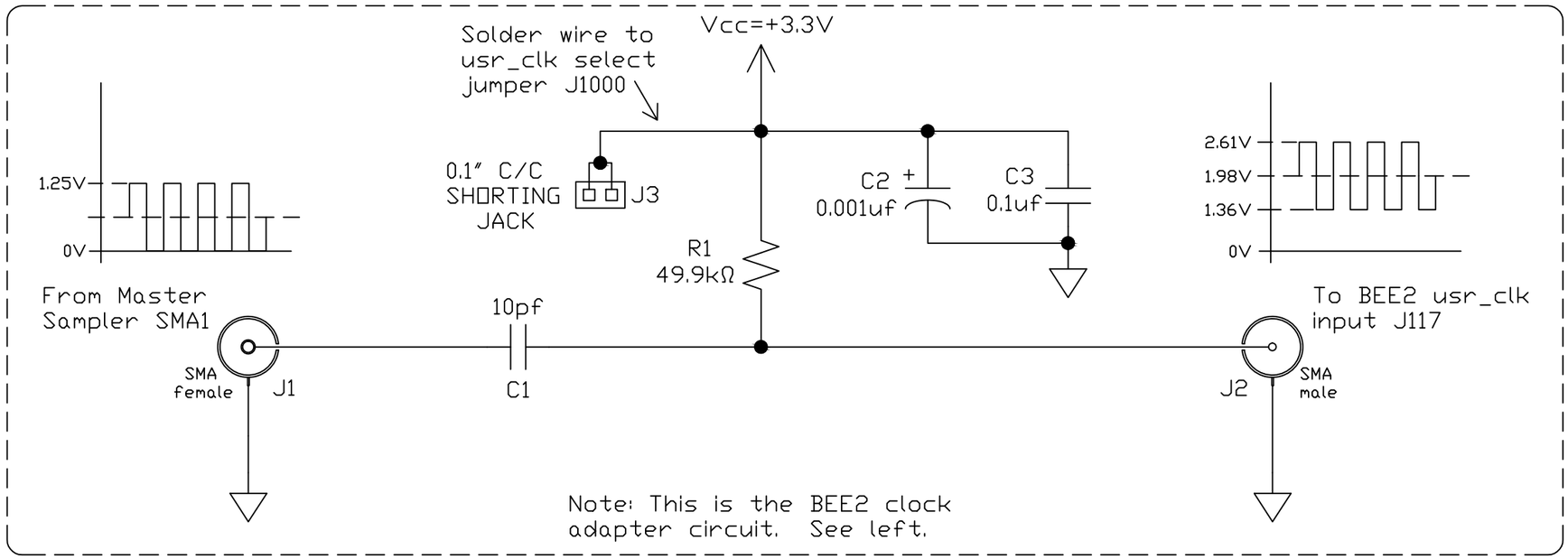




This circuit is required to adjust the signal outputs of the iBOB to match the signal input requirements of the BEE2 usr_clk circuit.

The iBOB SMA outputs are LVTTL, with signal levels of 0.00V to +1.25V

The BEE2 usr_clk interface has LVPECL inputs, with the following input signal requirements:

Vcc-1.165 < VIH < Vcc-0.880
or 2.135 < VIH < 2.420

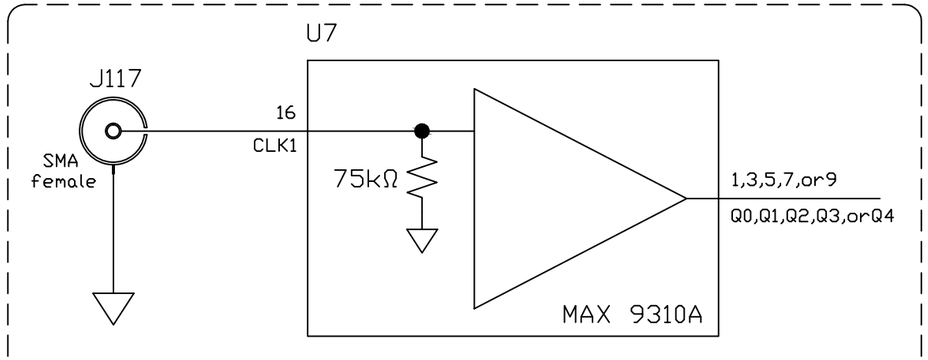
Vcc-1.810 < VIL < Vcc-1.475
or 1.490 < VIL < 1.825

The iBOB output signal is AC coupled with the 10pf capacitor, shifting the levels to -0.625V to +0.625V

The voltage divider created by R1 (49.9kΩ) to Vcc and the 75kΩ resistor (internal to U7) to GND sets the operating point to:

3.3 * (75k/(75k+49.9k)) = 1.982V

which provides signal levels of +1.355V to +2.605V, which satisfies the input requirements of the MAX 9310A.



NATIONAL RADIO ASTRONOMY OBSERVATORY P.O. BOX 2, GREEN BANK, WEST VIRGINIA, 24944					TOLERANCES UNLESS OTHERWISE SPECIFIED ANGULAR ±0°30' FRACTIONAL ±1/64 2 PLACE DECIMAL ±.01 3 PLACE DECIMAL ±.005 DIMENSIONS ARE IN INCHES
PROJECT/TITLE	GUPPI BEE2 CLOCK ADAPTER				
DESIGNED RLM	DRAWN JMR	CHECKED			DATE 08/31/10
SCALE	MATERIAL	FINISH			DRAWING NO. B45420S004
FILE \ARCHIVE\45420\S004	SHEET 1 OF 1	REVISION –			