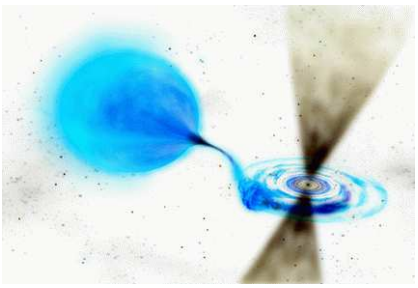

CICADA Note #2

Event Capture α Project Plan and Design Requirements

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ABSTRACT

Many applications of the FPGA based design of the CICADA project will benefit from a short duration event capture capability. This document specifies the requirements of the first event capture design. The design must fit within the IBOB board and enables capture of a block 8192 samples in each of two polarizations and make these samples available to linux computer, communicationig via the IBOB serial port.

Later specifications will include additional transient event detection modes, a spectral line mode and communication via the 10 Mbps Ethernet port on the IBOB.

Change Record

Revision	Date	Author	Sections/Pages Affected
	Remarks		
1.0	2007-July-03	G. Langston	All
	Initial version for the project planning meeting.		
2.0	2007-July-18	G. Langston	1-2
	Revise to include budget and staffing plan.		
2.1	2007-July-19	G. Langston	1-2
	Slight cost revision.		

1. Need and Feasibility

The event capture design described here is motivated by recent detections of pulsars from single events (e.g. McLaughlin *et al.*) and by serious efforts by a number of groups to detect Neutrinos via their radio wavelenght Cerenkov radation, when interacting with the material on the Lunar surface (Hankins *et al.* 1996).

Dan Wertheimer, of U.C. Berkeley, presented the capabilities hardware developed of the CASPER group for flexible design of hardware for high speed, broad bandwidth data acquisition. The NRAO CICADA group considered a number of possible first designs for development, and found the event capture design to be feasible.

The CASPER hardware consists of three main modules and a development environment for Xilinx code design. The modules are

ADC Analog to Digital converter. The converter can sample two input signals at a rate of up to 0.5 Giga-samples per second per input. The data are buffered on the ADC and provided to the downstream hardware in groups of two sets of four samples.

IBOB Interface board that accepts ADC data and performs limited initial processing. Data are communicated to other hardware via serial links, ethernet and 10 GBps ethernet protocols.

BEE2 High end data processing board. Processing is via 5 Xilinix chips and input and output are via 10 Gbps ethernet and XAUI interfaces.

2. Project Authorization

The event capture design is considered to be appropriate for student development, and the task was assigned to two summer students from WVU, Brandon Rumberg and Patrick Brandt. Since the project is a small scale effort, the project was authorized by Richard Prestage, after consultations with John Ford, Randy McCullough and Glen Langston.

3. Authorization for Phase

The project was considered small enough to be considered for full approval, including design, implementation, deployment and testing.

4. Project Scope

The design must fit within the IBOB baord and enables capture of a block 8192 samples in each of two polarizations and make these samples available to Linux computer, communicationig via the IBOB serial port.

The event capture will be triggered based on the input signal level in either of the two input RF data streams. The event to be captured will be in the *middle* of the captured data interval, allowing comparison of signal spectra before, during and after the event. The α design will record time via internal counters and synchronize the internal counters with external time by capturing the counter state at the time of detection of the rising edge of the external sync pulse. The α design will record the clock counters at the time of the events.

The design outputs are via the serial link, in response to queries from the Linux computer.

The α design will not use the ethernet link for communication to a Linux computer.

5. Sequence

The event capture α design is a learning tool for the development of future data acquisition systems. The development will be based on using parts of existing CASPER designs, particularly the **Pocket Spec** design, which has spectral line and data capture aspects.

6. Duration

The event capture project will have a duration of 12 weeks. The project plan builds on experience by the U. Cincinnati team with developing simulated designs for the IBOB board. In addition, the work done by Randy McCullough, John Ford, and Pam Ford in setting up the development environment was critical for allowing timely completion of the project.

The plan calls for two students to work two months on project design and development. In the third month, we will document the design and plan the β version of the event capture design. The project manager will work on this project approximately 1 day a week for the duration of the project.

7. Schedule

Week 1 The students will read the documentation and be given guided examples of developing IBOB designs using MATLAB and Simulink.

Week 2 Students will continue document reading, and experimenting with simple

IBOB designs.

Week 3 Initial design specification written and discussed with team members.

Week 4 Tasks divided between FGPA programming and Linux C programming for data display and recording.

Week 5 Study of Berkeley "Pocket Spec" design and consideration of modifications for use in Event Capture design.

Week 6 Initial Capture of test data events.

Week 7 First communication of events to Linux computer.

Week 8 First Operational tests of event capture using laboratory signals.

Week 9 Design modifications and debugging.

Week 10 Astronomical Testing connected to the 43m telescope IF chain.

Week 11 Documentation for FPGA design and Linux side data recording.

Week 12 Documentation Review at beginning of week 12, followed by updates of documentation for the remainder of time.

8. Cost Estimate

The project hardware are already acquired for a separate project, a spectral line detector for the 43m. The project hardware includes: *1)* the development computer, *2)* one ADC, *3)* one IBOB, *4)* IBOB power supply and interface cables, and *5)* Pair of amplifiers and filters to set input IF power. *6)* 1 Hz clock signal and high frequency clock (500 to 1000 MHz). *7)* Data acquisition computer. The total value of these components is $16,000. At the completion of this project, these components will be returned to their normal uses.

The software costs for MATLAB and SIMULINK development are significant. The total software cost is approximately $25,000. No dedicated licenses are required for the Event Capture project, and all installed software will be used for other FPGA development projects.

The staffing costs are the costs of hiring two summer students. These students will each work for 10 weeks. We estimate the Project manager will work one day a week for the project duration. The total FTE equivalent project manager week is 2 for this project. The project engineer will work a total of 1 week on the project over the duration of the project. The estimated salary cost for this project is $23,000.

9. Budget Plan

The incidental costs of the development budget plan will be born by the 43m Bi-static radar project as a part of the spectrometer development effort.

10. Staff

The project staff are Glen Langston, manager, Brandon Rumberg and Patrick Brandt programmer/designers, and John Ford, project engineer. Brandon and Patrick are students at WVU and will be employed by NRAO for Summer 2007.

11. Project Plan

Due to the small scope of this project, this document serves as the project plan.

12. Project Initiation

Because of the small scope of this project and the recognized need for NRAO to develop some expertise in FPGA design, the project was approved early, by Richard Prestage, for execution. The project was approved in April 2007.

13. Project Execution

The project began with the arrival of Brandon Rumberg to NRAO Green Bank on May 14, 2007. Patrick Brandt began the project work on May 28, 2007. After the intial introductory phase, the students worked independently on project development.

14. Project Control

The project control will be done via milestones, that will be scheduled to be completed approximately every two weeks during the execution phase.

Environment Before any development could begin, the MATLAB and SIMULINK systems were installed on the dedicated development computer. In our case the development was done in the Windows environment on computer `echo.gb.nrao.edu`.

Flash Lights The students will produce first simple IBOB designs that will flash the IBOB lights at regular intervals, thus demonstrating the capability of programming the IBOB.

FPGA Software The students will write special purpose test programs to demonstrate a knowledge of IBOB C language programming.

PocketSpec The Pocket spectrometer design was important for the event capture design, because it illustrated a method of capturing data and transferring the data to an external computer for examination and logging.

Initial Version The first event capture designs will be run in Simulink, without ADC hardware. These designs must be tested by loading in simulated events. These tests will all be done within the MATLAB/Simulink environment.

Linux Com. First first to communicate data to the Linux based, data acquisition computer. Communication is via the IBOB serial port.

Clocked Events First version to latch the IBOB internal clock to the event capture time.

Real Time Clock First version to capture the external, maser referenced, real time clock.

15. Project Closeout

The project will be closed out at the end of initial deployment of the system connected to the 43m IF chain. The project team must demonstrate collection of real data from the 43m telescope in both polarizations. The data must be plotted in intensity versus time order and a fourier transformed in four blocks. The blocks are: **A,B** data in each polarization obtained before the event and **C,D** data in each polarization obtained during the event. The event end will be determined by visual inspection of the time series.

REFERENCES

Hankins, T. H.; Ekers, R. D.; O'Sullivan, J. D., (1996), *A search for lunar radio Cerenkov emission from high-energy neutrinos*, *MNRAS*, **283**, 1072.

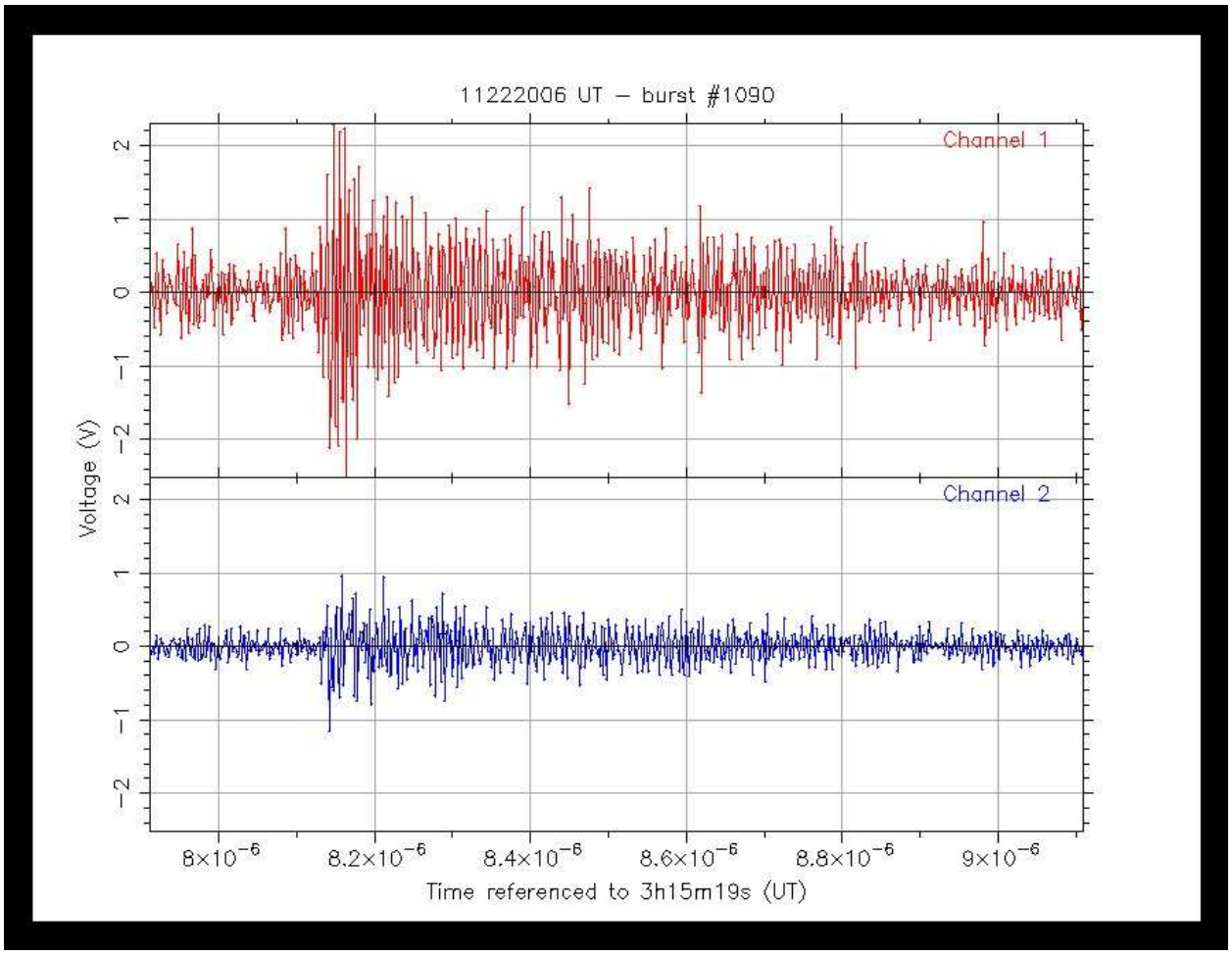

Fig. 1.— Event captured by Rich Bradley, Erin Mastrantonio and Glen Langston, from a 43m observation on November 22, 2006. The observations were made as a test of the possibility of using the 43m telescope to capture short duration events. The X axis in both plots is time. The total duration of the event capture was 16 μseconds. The Y axis is intensity for X and Y polarizations. The center frequency of the observation was 800 MHz and the bandwidth was 200 MHz.

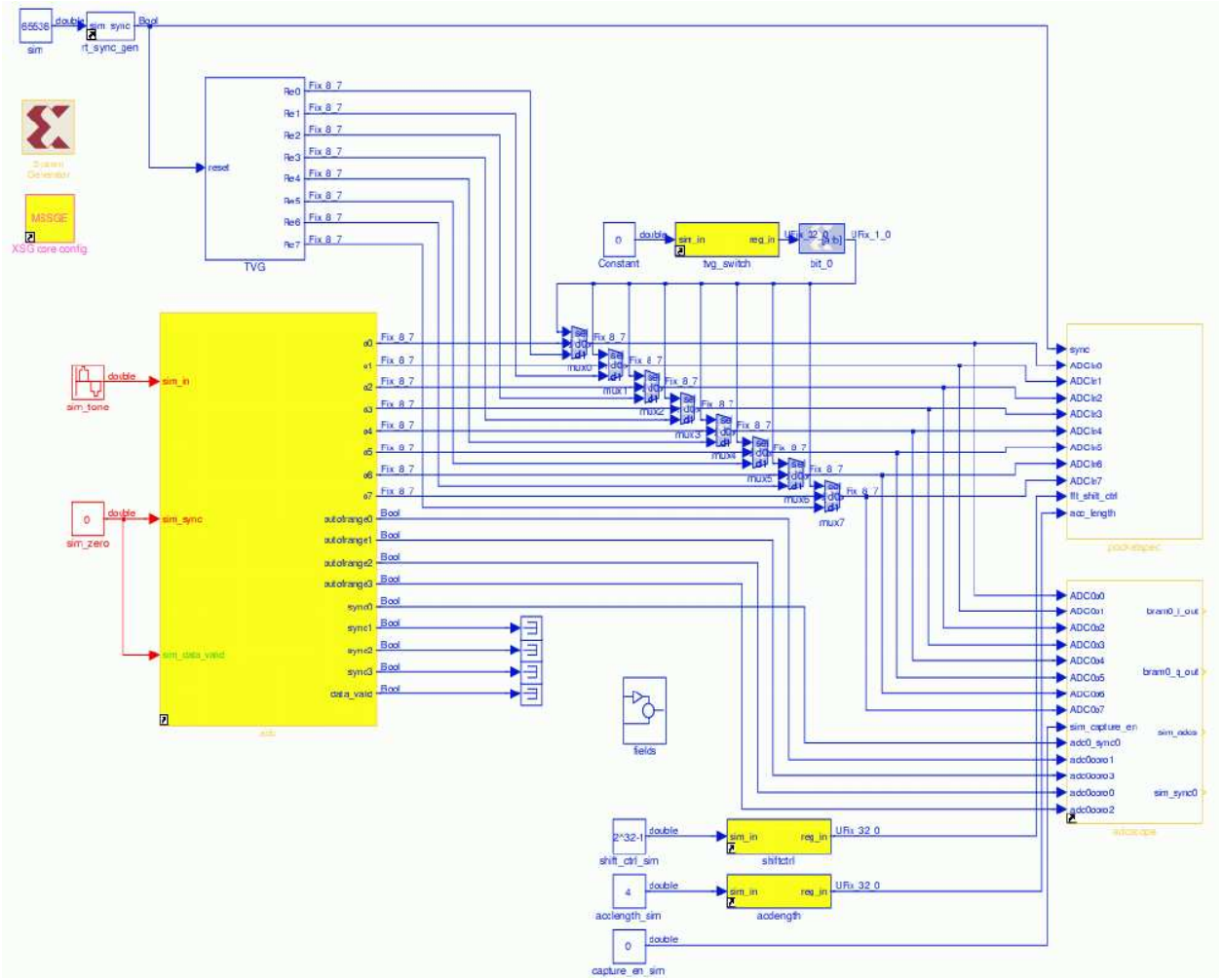

Fig. 2.— The CASPER pocket Spectrometer design in the MATLAB development environment. Review of this design was the first goal of the event capture team.